297-1771-550

Digital Switching Systems

DMS-Spectrum Peripheral Module

Hardware Maintenance Reference Manual

DMSSPM15 Standard 05.02 April 2001

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Standard 05.02 SP15 (CSP15). Added/changed the following for the release:

- Added the NTLX91BA SPM-DMS frame assembly
- Added notes relate to the NTLX63AA CEM not being compatible with SP15 or later
- SR NR10722 removed the following alarms from Chapter 2, “Visual alarm indicators”:
  - CSS
  - CV
  - CVFE
  - ES
  - ESFE
  - LBC
  - OPT
  - OPR
  - SEFS
  - SES
  - SESFE
  - UAS
  - UASFE

February 2001

Standard 05.01 SP15 (CSP15). Added/changed the following for the release:

- Added the NTLX82BA CEM per features 59018984 and 59019804.
- Made editorial changes to Chapter 1, “Introduction”, and Chapter 2, “Visual alarm indicators.”
- Made the following changes to Chapter 3, “Hardware descriptions:”
  - — Modified the resource modules listed in the “NTLX51AA dual-shelf assembly” and “NTLX51BA dual-shelf assembly”
  - — Modified the suggested locations listed in the “NTLX65BA DSP RM”, “NTLX66BA VSP RM”, “NTLX72AA DLC RM”, and “NTLX85/86AA VSP RM.”
  - — Made editorial updates to reflect the suggested use of the NTLX51BA dual-shelf assembly over the NTLX51AA.

October 2000

Standard 04.03 SP14 (CSP13/14). Updated the NTLX51AA and NTLX51BA dual-shelf assemblies per SR 10366713.

August 2000

Standard 04.02 SP14 (CSP13/14). Released due to late SME comments.

August 2000

Standard 04.01 SP14 (CSP13/14). Updated the DSP RM provisioning guidelines per SME’s email dated July 27, 2000.

June 2000

Standard 03.05 SPM12 (CSP12). Updated the NTLX85/86AA VSP RM section per SR 10343869.

February 2000

Standard 03.04 SPM12 (CSP12).

- Made revisions to the ATM RM, NTLX73AA
- Made revisions to the DLC RM, NTLX72AA
- Made revisions to the OC3 RM, NTLX71BA
- Added the NTLX51BA dual-shelf assembly

February 2000

Standard 03.03 SPM12 (CSP12). Added optical interface specifications to the OC3 RM section of the document per SR CH90186.

January 2000

Standard 03.02 SPM12 (CSP12).

- Made revisions to the CEM RM, NTLX82AA.
- Included the ATM RM, NTLX73AA.
- Added the DLC RM, NTLX72AA.

December 1999

Preliminary 03.01 SPM12 (CSP12).

August 1999

Upissued to Standard 02.03 SPM11 (CSP11) to add NTLX82AA common equipment module (CEM) based on SR NV90426.

July 1999

Standard 02.02 SPM11 (CSP11).

The information regarding the NTLX73AA asynchronous transfer mode (ATM) resource module (RM) has been moved to the “ATM General Description," 297-1771-150.

Made editorial changes.

June 1999

Preliminary 02.01 SPM11 (CSP11).

- Feature AF7378 added hardware procedure for ATM RM, NTLX73AA.
- Made editorial changes

February 1999

Standard 01.05 SPM01 (CSP09). Changed the product name to "DMS-Spectrum Peripheral Module (SPM)." Added information about DSP provisioning to the “NTLX65AA DSP RM."

October 1998

Standard 01.04 is the initial release for SPM01 (CSP09).

Contents

About this document

When to use this document

Use this document when you need maintenance information about the hardware components of the DMS-Spectrum Peripheral Module (SPM).

Audience and applicability

This document provides information for operating company personnel responsible for SPM installation, provisioning, and maintenance. This manual also provides information for others who are interested in a general description of the SPM features and hardware.

How to check the version and issue of this document

The version and issue of the document are indicated by numbers, for example, 01.01.

The first two digits indicate the version. The version number increases each time the document is updated to support a new software release. For example, the first release of a document is 01.01. In the *next* software release cycle, the first release of the same document is 02.01.

The second two digits indicate the issue. The issue number increases each time the document is revised but released again in the *same* software release cycle. For example, the second release of a document in the same software release cycle is 01.02.

This document is written for all DMS-100 Family offices. More than one version of this document may exist. To determine whether you have the latest version of this document and how the documentation for your product is organized, check the release information in *Product Documentation Directory*, 297-8991-001.

You should be familiar with the DMS system and DMS peripheral modules (PM) before you attempt to use the information in this manual.

Related NTPs

Refer to the following documents for more information about SPM:

- *DMS-Spectrum Peripheral Module Service Implementation Guide*, 297-1771-301.
- *DMS-Spectrum Peripheral Module Feature Description Reference Manual*, 297-1771-330.

- *DMS-Spectrum Peripheral Module Commands Reference Manual*, 297-1771-819.
- SPM information is also included in the following NTPs:
  - *Trouble Locating and Clearing Procedures*
  - *Alarm Clearing Procedures*
  - *Recovery Procedures*
  - *Routine Procedures*
  - *Card Replacement Procedures*
  - *Operational Measurements*
  - *Data Schema*
  - *Logs*

1 Introduction

The DMS-Spectrum Peripheral Module (SPM) is functionally equivalent to a digital trunk controller for interswitch trunks. It provides common channel signaling #7 and per-trunk signaling speech and data trunks on TR-782 compliant Optical Carrier 3 (OC3) carriers. Internally, all trunks are treated as DS-0s or as sets of DS-0s.

As shown in the following figure, the NTLX91BA frame assembly contains two NTLX51AA or NTLX51BA dual-shelf assemblies (two complete SPMs) and the necessary support equipment. Each dual-shelf assembly provides 30 slots to accommodate

- two NTLX61AA shelf interface modules (SIM)—one SIM needs to be one each shelf on the dual-shelf assembly
- two NTLX63AA, NTLX82AA, or NTLX82BA common equipment modules (CEMs) for each dual-shelf assembly

  Note: The NTLX63AA CEM is not compatible with SP15 or later.

- two NTLX71AA or NTLX71BA OC3 interface modules for each dual-shelf assembly
- two NTLX72AA data link controller (DLC) RMs for each dual-shelf assembly
- 0 to 24 NTLX65AA or NTLX65BA digital signal processor (DSP) resource modules (RMs) or NTLX66AA, NTLX66BA, NTLX85AA, or NTLX86AA voice signal processor (VSP) RMs for each dual-shelf assembly

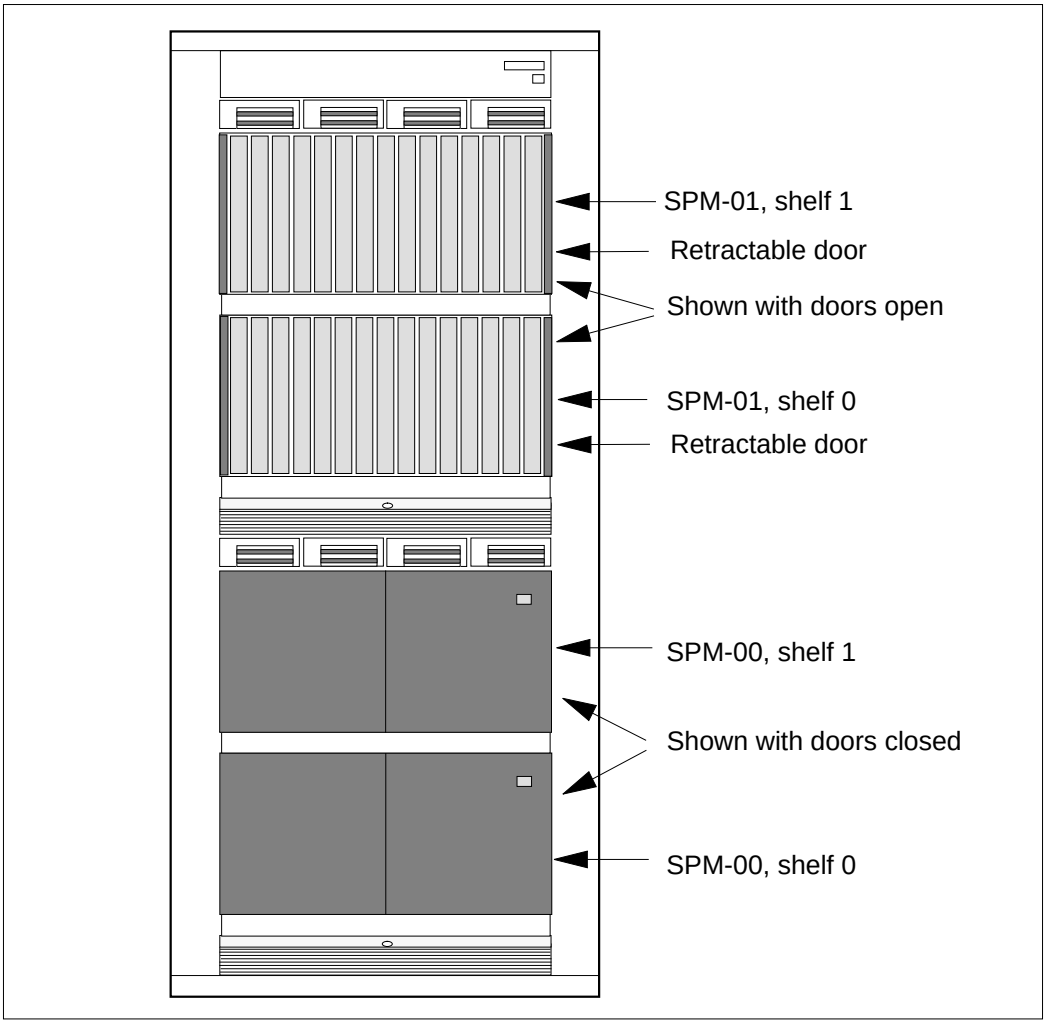
  Note: Support exists for any combination of up to 24 DSP and VSP RMs. Typically, the number of necessary DSP and VSP RMs will be less than this.

ATTENTION
Not all modules apply to all markets.

The NTLX55AA cooling unit provides forced-air cooling to the SPM equipment by four NTLX56AA fan assemblies.

The NTLX57 PCIU serves as a central gathering point for all power and alarm cabling used within the NTLX91BA frame assembly.

The NT9X40DA paddleboard provides the SPM interface to the DMS switch and the enhanced network (ENET). The paddleboard supports four SPM DS-512 connections to the ENET.

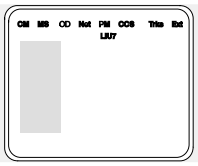


2 Visual alarm indicators

The DMS-Spectrum Peripheral Module (SPM) frames and modules have visual alarm indicators, which are connected to the DMS aisle alarm indicators.

MAP terminal

The MAP terminal displays the following alarm.



CM	MS	IOD	Net	PM	CCS	Lns	Trks	Ext	APPL
.	.	.	.	.	.	.	.	.	.

If an alarm is reportable and a higher level alarm does not mask it, the alarm indicator appears under the peripheral module (PM) category of the alarm banner on the MAP terminal.

Alarm indicators consist of two lines that include the following elements:

- *xxyyy*
- *zzz*

xx: represents the number of the SPM unit with at least one alarm of the same severity

yyy represents the type of device, which is always SPM for SPM units

zzz represents one of the following severity codes

- **C** — critical alarm
- *M* — major alarm
- <blank> — minor alarm
- — no alarm

A higher level alarm masks all levels below it. For example, a critical (*C*) alarm masks both major (M) and minor ( ) alarms. If lower level alarms are present, they are reported in a log.

When there are no alarms, a dot (•) appears in the device field (xxyyy).

List command

You can display a list of the alarms at all levels using the LISTALM command.

Logs

Each reportable alarm generates a log containing information about the alarm.

SPM alarm classifications

There are three different causes of SPM alarms, and these alarms are reported by various devices. These devices can be part of the SPM or part of the DMS alarm reporting system.

The following can cause SPM alarms:

- device failures
- network events
- threshold crossings

The following can report SPM alarms:

- an SPM network node
- individual SPM modules
- the DMS computing module (CM), which reports alarms for
  - — input/output devices (IOD)
  - — common channel signaling (CCS)
  - — trunks (TRKS)
  - — carriers (CARR)

Device failures

Physical devices generate alarms when a detectable failure occurs. SYSBNA is an example of this type of alarm.

Network events

Various sources generate network-event alarms when monitored events occur on the network. AIS and LOS are examples of this type of alarm.

Threshold crossings

Alarms generate when monitored parameters or metered parameters exceed their datafilled settings. SPM devices or network events, or both, can cause these alarms. COTLOW and VCXO70 are examples of these types of alarms.

SPM network node

An SPM node consists of all the modules on shelves 0 and 1, which connect to the OC-3 network through the OC-3 modules in slot 9 and slot 10 on shelf 0.

SPM modules

The following SPM modules can generate alarms:

- common equipment module (CEM)
- OC-3 interface module (OC-3)
- DLC interface module (DLC)
- digital signal processor (DSP)
- voice signal processor (VSP)

Note: The VSP does not apply to all markets.

DMS computing module

SONET carriers can generate alarms at the following DMS computing module (CM) alarm reporting levels:

- trunks (Trks)
- input/output devices (IOD)
- common channel signaling (CSS)

Threshold-crossing alarms

The SPM CEM and the DMS CM can generate threshold-crossing alarms. Threshold-crossing alarms are one of the following types:

- steady-state faults
- performance parameters
- metered-performance parameters

You can enter high-threshold and low-threshold values for the various alarms in DMS data schema tables. Refer to the *Data Schema Reference Manual* or the data schema section of the *Translation Guide*, as appropriate. Alarms generate when the high-value threshold is crossed and they clear when the low-value threshold is crossed. See the alarm descriptions for the appropriate data schema table references.

Steady state faults

Steady state faults, or soaked defects, occur when a performance parameter crosses an upper threshold and remains above the lower threshold value for an extended period. AIS and RFI are examples of steady-state fault alarms.

Performance parameters

Performance parameters are counts of intermittent defects. Alarms generate when counts exceed threshold values. Performance parameters are collected over 15-minute periods and 1-day periods. Performance parameter counts are reset when collection periods end. CV and ES are examples of performance parameter alarms.

Metered performance parameters

Metered performance parameters are physical measurements. Alarms generate when a measured value exceeds its benchmark setting by the datafilled percentage. Benchmark settings can be reset. LBR and OPT are examples of metered performance parameter alarms.

Significance of alarm indicators

Alarm indicators are LEDs that appear at the top of each frame and at the top of the faceplate on each SPM module. All modules have a red and a green module-status indicator. Modules with external connections on the faceplate also have an additional amber signal-status indicator, which indicates the status of the external connections.

See the following tables for information about the significance of individual alarm indicators and alarm-indicator combinations.

Table 1

Module-condition LED combinations		
Green	**Red**	**Indication and action**
Off	Off	Green LEDs are in sleep mode (module can also be not powered or not seated). When all LEDs are off, there are no critical faults and an indicator test is not underway. Use an indicator test to check LED function.
On	On	A power on self test (POST) or an LED indicator test is underway. During a POST, the LEDs are controlled by the initial boot loader (IBL) software. If both LEDs remain on for an extended period after a POST, the module is defective. For detailed instructions for replacement, see the appropriate *Card Replacement Procedures*.
On	Off	Normal operation—there are no critical faults and no action is required. Do not remove a module displaying this alarm-indicator combination.
Off	On	Critical fault—replace the module.
Note: To prolong LED life, program the green LEDs so it can enter the sleep mode. LED sleep-mode timing is controlled by the entry in field LEDTIMER in data schema table MNNODE. Sleep mode does not apply to red LEDs.		

Table 2

External signal-status LEDs	
Amber	**Indication**
Off	Normal operation—all external signal inputs to the module faceplate are valid.
On	At least one external signal source entering the module faceplate is not carrying a valid signal.
Note: Sleep mode does not apply to amber LEDs.	

Note: Alarm indicators do not indicate maintenance states (such as manual busy, in service, or in service trouble) or activity states (active or inactive).

SPM alarms

The following table lists the alarms for the SPM and indicates the resource or control parameter generating the alarm.

Table 3 (Sheet 1 of 2)

Source device or parameter									
AlarmName	**SPM Node**	**CEM**	**OC-3**	**DSP**	**VSP**	**DLC**	**DMS TRKS**	**CARR METER**	**CARR PERF**
Alarms appearing under the PM banner									
CLKOOS		X							
COTLOW	X								
DTMFLOW	X								
ECANLOW	X								
HLDOVR		X							
HLDOVR24		X							
MANB	X	X	X	X	X	X			
MANBNA	X	X	X	X	X	X			
MFLOW	X								
ISTB	X	X				X			
NOSPARE			X	X	X	X			
PROTFAIL			X	X	X	X			
SYSB	X	X	X	X	X	X			
SYSBNA	X	X	X	X	X	X			
TONESLOW	X								
VCXO70		X							
VCXO90		X							
Alarms appearing under the TRKS banner									
AIS							X		
BERSD							X		
BERSF							X		

Table 3 (Sheet 2 of 2)

Source device or parameter									
AlarmName	**SPM Node**	**CEM**	**OC-3**	**DSP**	**VSP**	**DLC**	**DMS TRKS**	**CARR METER**	**CARR PERF**
LOF							X		
LOP							X		
LOS							X		
RAI							X		
RFI							X		
SIMPLEX							X		

3 Hardware descriptions

This chapter describes the hardware components of the DMS-Spectrum Peripheral Module (SPM). The component descriptions follow a top-to-bottom order. The chapter describes the following components:

- NT9X40DA paddleboard
- NTLX50AA SPM-DMS frame assembly

  Note: The NTLX50AA SPM-DMS frame assembly is not compatible with releases after SP11.

- NTLX51AA dual-shelf assembly
- NTLX51BA dual-shelf assembly
- NTLX55AA cooling unit and grill assemblies
- NTLX57AA PCIU
- NTLX60AA filler module
- NTLX61AA shelf interface modules (SIM)
- NTLX63AA common equipment modules (CEM)

  Note: The NTLX63AA CEM is not compatible with SP15 or later.

- NTLX65BA DSP RM
- NTLX66BA VSP RM
- NTLX71BA OC-3 interface module
- NTLX72AA DLC RM
- NTLX82AA common equipment modules (CEM)
- NTLX82BA common equipment modules (CEM)
- NTLX85AA and NTLX86AA VSP RM
- NTLX91BA SPM-DMS frame assembly

Note: Not all modules apply to all markets.

NT9X40DA paddleboard

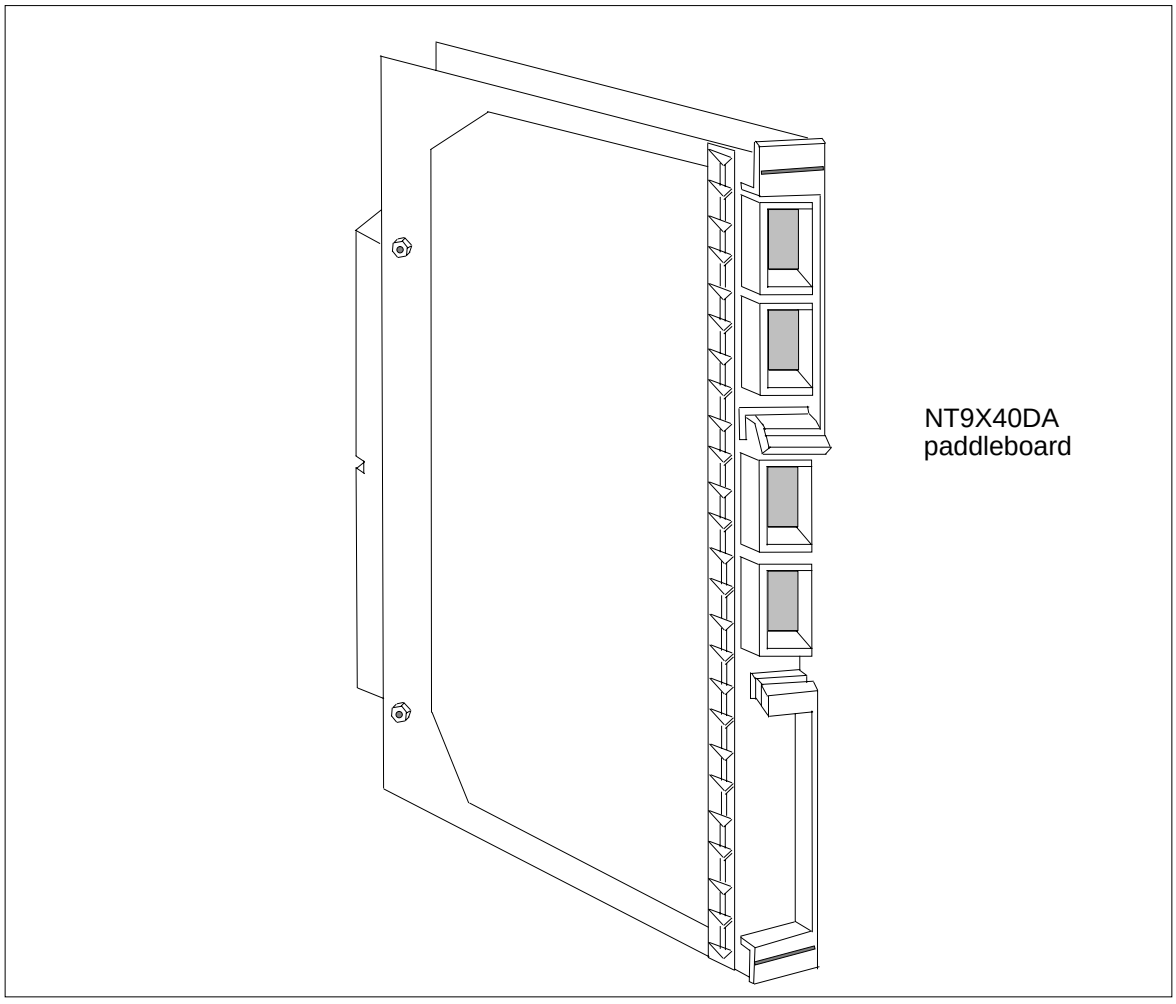
Description

The DMS-Spectrum Peripheral Module (SPM) uses the NT9X40DA paddleboard to interface with the DMS switch through the enhanced network (ENET) crosspoint (XPT) card.

The NT9X40DA ENET quad DS-512S fiber link interface is one of several SuperNode or SuperNode SE ENET paddleboards. The NT9X40DA paddleboard uses four hard-clad silica (HCS) fibers operating at 650 nm wavelength to provide 2048 channels to the ENET XPT cards.

The NT9X40DA is the only network interface paddleboard that currently supports hard-clad silica fiber and it cannot be substituted for any of the other fiber link interface paddleboards such as the NT9X40BA or the NT9X40BB.

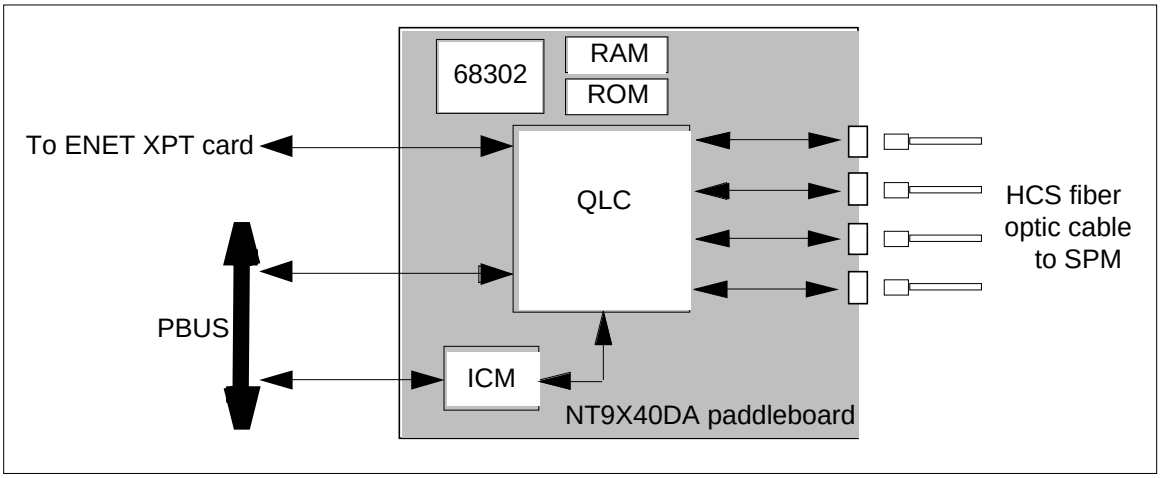
NT9X40DA paddleboard (continued)



Location

As shown in the following figure, the NT9X40DA ENET paddleboard resides in the ENET shelf and connects to the common equipment module (CEM) in the SPM using HCS fiber-optic cable.

NT9X40DA paddleboard (continued)



Dependencies

The DMS message switch (MS) must have a minimum of the following items to provide the ENET functionality required by the SPM connected to the NT9X40DA paddleboard:

- NT9X13DC, MS CPU Processor CP (4 Mbytes)
- NT9X17DA, MS 64-Port CP
- NT9X20BB, ENET/MS Fiber Interface PB
- NT9X25AA, MS Port Expander PB
- NT9X25BA, MS Port Expander/Terminator PB
- NT9X49CB, MS P-Bus Terminator CP (Tracer Card)

Note 1: To interface with the ENET, the MS requires 10 Mbytes of memory.

Note 2: The NT9X25AA and NT9X25BA are required only if a chain of NT9X17DAs are installed.

Note 3: A 128-port NT9X17CA card must be paired with an 9X20BC card.

Features

The NT9X40DA paddleboard provides the following features:

- lower cost electro-optic modules and connectors
- easy cable termination
- smaller bend radius of HCS fiber

- duplex keyed connector (no reversing RX and TX)
- simpler connect and disconnect action
- visible wavelength
- embedded maintenance channel
- alarm codes replaced by status bits
- embedded cycle redundancy checking (CRC)
- enhanced reset capability
- more robust and more integrated clock recovery

Functions

The NT9X40DA paddleboard provides the following:

- four DS-512S fibers
- 2048 channels
- 16-bit CRC
- ENET shelf processor access to the processor bus (PBus)

Functional blocks

NT9X40DA paddleboard consists of the following functional blocks:

- fiber interface and quad link chip (QLC)
- pad connection memory using integrated connection memory (ICM)
- 68302 integrated processor
- PBus interface

Fiber interface and the quad link chip (QLC)

The fiber interface and the QLC provide

- four DS-512S fiber transmit/receive pairs
- multiplexed frame channel
  - — out-of-band maintenance and messaging
  - — facility data link (FDL) channel
- local processor interface
- maintenance and messaging internal registers
- full frame elastic store for each DS-512S receive link
- pseudo-random bit sequence (PRBS) data insertion and extraction

NT9X40DA paddleboard (continued)

- CRC-16 error correction
- 2048, 10-bit ENET channels

Pad connection memory

The pad connection memory uses an ICM to provide ±7 dB DS-0 pads that are adjustable in 1 dB steps. The ICM is used as the gain or loss pad connection memory.

Integrated processor

The 68302 integrated processor block contains a central processing unit (CPU), a flash read-only memory for CPU firmware, and static RAM for incoming and outgoing message storage. The integrated processor performs the following major functions as well as other minor functions:

- inserts the FDL message information protocol
- responds to QLC interrupts
- stores messages in transit between the ENET shelf processor and the CEM

PBus interface

The PBus provides the bus connection to the ENET shelf processor and shelf processor access to the identification programmable ROM.

Signaling

The following table shows power pin numbers.

Pin number	Signal	Function	Description
26A, 29A, 32A, 37A, 38A, 43A, 48A, 53, 59A, 59B, 59C, 65A, 65B, 65C, 65D	GND	power	Logic ground
27A, 28A, 30A, 31A, 39A, 40A, 41A, 42A, 44A, 45A, 46A, 47A, 49A, 50A, 51A, 52A	+5.0 V	power	+5.0 volts power supply
33A, 34A, 35A, 36A	-5.2 V	power	-5.2 volts power supply

NT9X40DA paddleboard (continued)

The following table shows the clock pin numbers.

Pin number	Signal	Function	Description
46D, 47D	CK21P+, CK21P-	input	49.152 MHz DS-512S clock, provided by the 9X35 crosspoint card.
48D, 49D	NFP21P+, NFP21P-	input	System frame pulse (active low) 8 kHz provided by the 9X35 crosspoint card frame pulse.
50D	CK61	input	16.384 MHz system clock
51D	NFP61	input	System frame pulse (active low) 8 kHz, frame pulse width one CK61 clock cycle
52D	NTFP61	input	System transmit frame pulse (active low) 8 kHz, frame pulse width on CK61 clock cycle

The following table shows the processor interface signal pin numbers.

(Sheet 1 of 2)

Pin number	**Signal**	**Function**	**Description**
39C, 39B	ADDR00, ADDR01	TTL input	Least significant processor address bits decoded from the byte enable strobes on NT9X36BA
40C,40B, 41C, 41B, 42C, 42B, 43C, 43B	ADDR02, ADDR03, ADDR04, ADDR05, ADDR06, ADDR07, ADDR08, ADDR09	TTL input	Processor address bus from the NT9X13KA
26D, 27D, 28D, 29D, 30D, 31D, 32D, 33D	DATA24, DATA25, DATA26, DATA27, DATA28, DATA29, DATA30, DATA31	TTL I/O	Processor data bus
37B	NDAS	TTL input	Processor delayed address strobe, active low
36B	RNW	TTL input	Processor read/write control. low=write
36C	NBPRST	TTL input	Reset from NT9X36BA, active low

NT9X40DA paddleboard (continued)

(Sheet 2 of 2)

Pin number	Signal	Function	Description
38C	NMPE	TTL input	Maintenance page enable, address strobe, active low
38B	NSPE	TTL input	SUDS page enable, address strobe, active low
44D	NCSEN	TTL input	Card slot enable, active low

The following table shows the network interface signal pin numbers.

Pin number	Signal	Function	Description
26C, 26B, 27C, 27B, 28C, 28B, 29C, 29B, 30C, 30B	RDAT0, RDAT1, RDAT2, RDAT3, RDAT4, RDAT5, RDAT6, RDAT7, RDAT8, RDAT9	TTL output	Receive bus from paddleboard, 16 Mbit/s, 10-bit wide, PCM data bus, 2048 channel capacity
31C, 31B, 32C, 32B, 33C, 33B, 34C, 34B, 35C, 35B	WBUS0, WBUS1, WBUS2, WBUS3, WBUS4, WBUS5, WBUS6, WBUS7, WBUS8, WBUS9	TTL input	Write bus to paddleboard, 16 Mbit/s 10-bit wide, PCM data bus, 2048 channel capacity

Power requirements

The NT9X40DA paddleboard power requirements are itemized in the following table.

(Sheet 1 of 2)

Parameter	Minimum	Nominal	Maximum	Units	Description
Supply voltage	4.75	5.00	5.25	V	5.0 V TTL logic
	-5.45	-5.20	-4.95	V	-5.2 V ECL logic
	3.23	3.30	3.37	V	QLC application specific integrated circuit (ASIC) supply voltage
Supply ripple			100	mV	

NT9X40DA paddleboard (end)

(Sheet 2 of 2)

Parameter	Minimum	Nominal	Maximum	Units	Description
Supply current; -5.2 V				mA	
Supply current; 5.0 V					
Supply current; 3.3 V					

NTLX50AA SPM-DMS frame assembly

Description

In the North American market, DMS-Spectrum Peripheral Module (SPM) equipment installs in a standard DMS NTLX50AA frame assembly. The DMS NTLX50AA frame is normally provisioned to accommodate two SPM nodes, although it can be used in a single node configuration. The module allows for expansion by adding circuit packs, cabling, and power.

ATTENTION
The NTLX50AA frame assembly is only supported by SP11 and earlier releases. For SP12 or later releases, use the NTLX91BA frame assembly.

The NTLX50AA frame assembly consists of the following features:

- standard DMS racks
- adapter brackets for dual-shelf assemblies
- cable segregation for power, fiber, signaling, and alarms
- accommodation of fiber bends of 1.5-in. radius
- front access for all cabling and maintenance activities
- retractable doors for cable protection
- covers for cable trough areas
- compatibility with DMS earthquake anchors and systems:
  - — earthquake-designed frame
  - — earthquake anchors
  - — earthquake bracing frames
- compatibility with overhead and under-floor DMS cabling systems
- Bellcore standards for electrostatic discharge (ESD) protection (ESD grounding is not required)

Components

As shown in the following figure, the NTLX50AA DMS frame assembly contains the following SPM equipment and component assemblies:

- NTLX51AA or NTLX51BA dual-shelf assembly
- NTLX57AA power cabling interface unit (PCIU)
- NTLX5015 air filter

- NTLX5010 upper grill
- NTLX5011 lower grill
- NTLX55AA forced-air cooling unit
- NT0X25BE gray framework

NTLX51AA dual-shelf assembly

One dual-shelf assembly provides 30 slots for the SPM plug-in modules. There are two NTLX51AA dual-shelf assemblies in each NTLX50AA gray framework assembly.

The NTLX51AA dual-shelf assembly accommodates the following items:

- NTLX5201 double-height backplane assembly
- NTLX5101 SPM shelf mechanical assembly (one for each dual-shelf assembly)
- NTLX5016 air-filter tray assembly
- NTLX5102 shelf-door kit
- NTLX5104 shelf cable-trough cover assembly

NTLX51BA dual-shelf assembly

One dual-shelf assembly provides 30 slots for the SPM plug-in modules. There are two NTLX51BA dual-shelf assemblies in each NTLX50AA gray framework assembly.

The NTLX51BA dual-shelf assembly accommodates the following items:

- NTLX5211 double-height backplane assembly
- NTLX5101 SPM shelf mechanical assembly (one for each dual-shelf assembly)
- NTLX5016 air-filter tray assembly
- NTLX5102 shelf-door kit
- NTLX5104 shelf cable-trough cover assembly

NTLX57AA PCIU assembly

The PCIU assembly accommodates a maximum of eight #6 AWG power cables from the power distribution center and 16 #10 AWG power cables for the termination of the shelf power supplies, as well as the required A and B returns.

NTLX50AA SPM-DMS frame assembly (continued)

The NTLX57AA PCIU assembly contains the following items:

- NTLX58AA alarm card assembly (one alarm card for each PCIU assembly)
- NTLX59AA fan management unit assembly (two fan management units for each PCIU assembly)

NTLX5015 air filter assembly

The air filter assembly filters the air supply for the NTLX51AA dual-shelf assembly. There are two NTLX5015 air-filter assemblies for each NT0X25BE gray framework assembly. The air-filter foam-element replacement part-number is A0665487.

NTLX5010 upper grill assembly

The upper grill assembly is located mid-point on the framework assembly. There is one NTLX5010 upper grill assembly for each NT0X25BE gray framework assembly.

NTLX5011 lower grill assembly

The lower grill assembly is located at the bottom of the framework assembly. There is one NTLX5011 lower grill assembly for each NT0X25BE gray framework assembly.

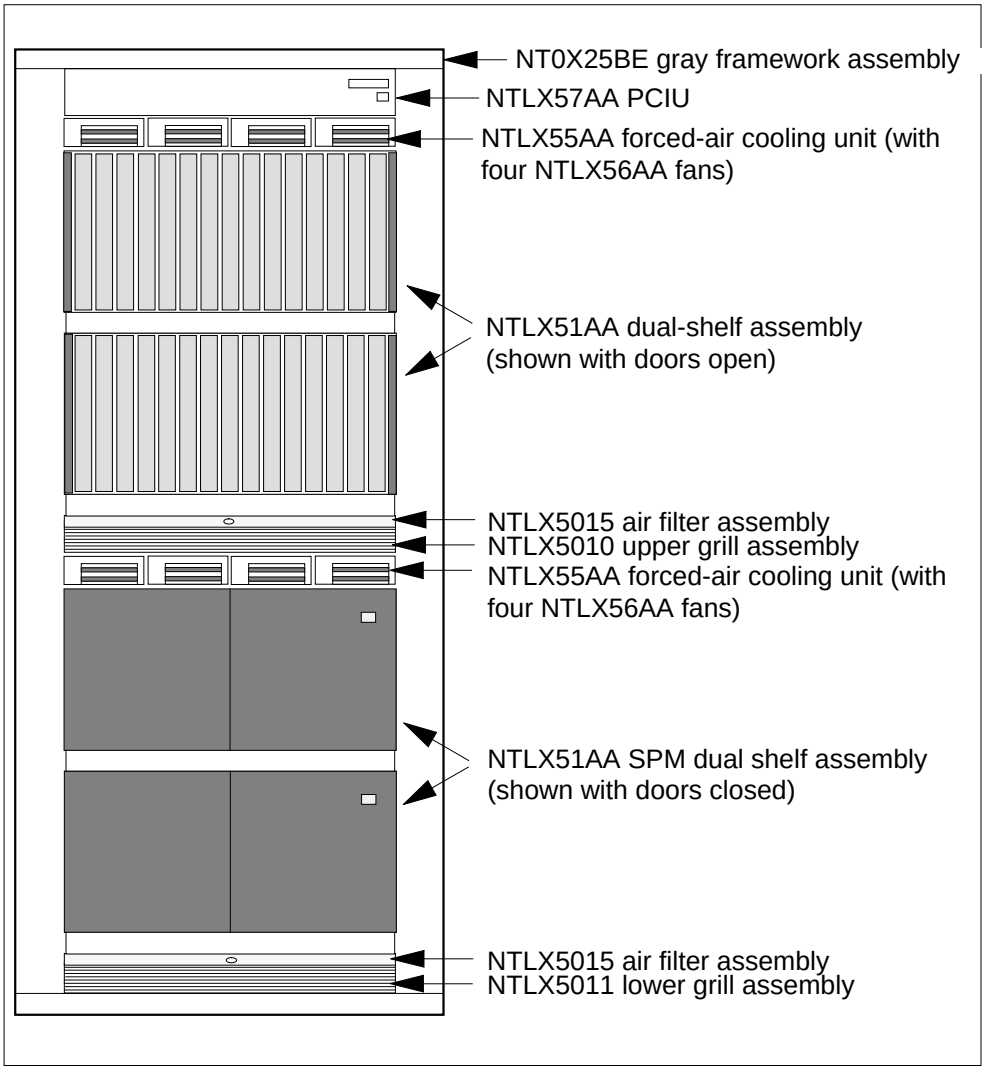
NTLX55AA cooling unit assembly

The cooling unit assembly provides mechanical ventilation for each NTLX51AA dual-shelf assembly. Each NTLX55AA cooling unit assembly contains four NTLX56AA fan assemblies.

NT0X25BE gray framework assembly

The NT0X25BE gray framework assembly consists of the frame that contains the built-in cable ducts, covers, and provides support for all the SPM components. There is one NT0X25BE gray framework assembly for two SPM nodes.

NTLX50AA SPM-DMS frame assembly (continued)



Frame cabling

All the external frame cabling and all inter-assembly internal frame cabling is accessible from the front of the NTLX50BE frame assembly.

NTLX50AA SPM-DMS frame assembly (continued)

Inter-assembly internal frame cabling

The cables listed in the following table connect the assemblies contained in the NTLX50AA frame.

Function	PEC	Connects	To
PCIU to SIM 1	NTLX5094	NTLX57AA PCIU	NTLX61AA SIM on the lower section of the bottom shelf
PCIU to SIM 2	NTLX5095	NTLX57AA PCIU	NTLX61AA SIM on the upper section of the bottom shelf
PCIU to SIM 3	NTLX5096	NTLX57AA PCIU	NTLX61AA SIM on the lower section of the top shelf
PCIU to SIM 4	NTLX5097	NTLX57AA PCIU	NTLX61AA SIM on the upper section of the top shelf
PCIU to cooling unit number 1	NTLX5098	NTLX57AA PCIU	NTLX55AA lower cooling unit assembly
PCIU to cooling unit number 2	NTLX5099	NTLX57AA PCIU	NTLX55AA upper cooling unit assembly
Frame ground cable	NTRX1650	NTLX50AA	Ground

External frame cabling

The external cables listed in the following table connect the NTLX50AA frame to other devices.

(Sheet 1 of 2)

Function	PEC	Number shown in figure	Number of cables	Wire type	Destination
-48 V dc and -48 V dc return	NPS9508-03-6	1	8	#6 AWG	Power distribution cabinet (PDC)
Alarm battery supply	NPS9508-03-14	2	1	#14 AWG	Next frame
Note: The NTLX81AA Fiber Adapter Kit is shipped loose—one kit for each OC3 module.					

NTLX50AA SPM-DMS frame assembly (continued)

(Sheet 2 of 2)

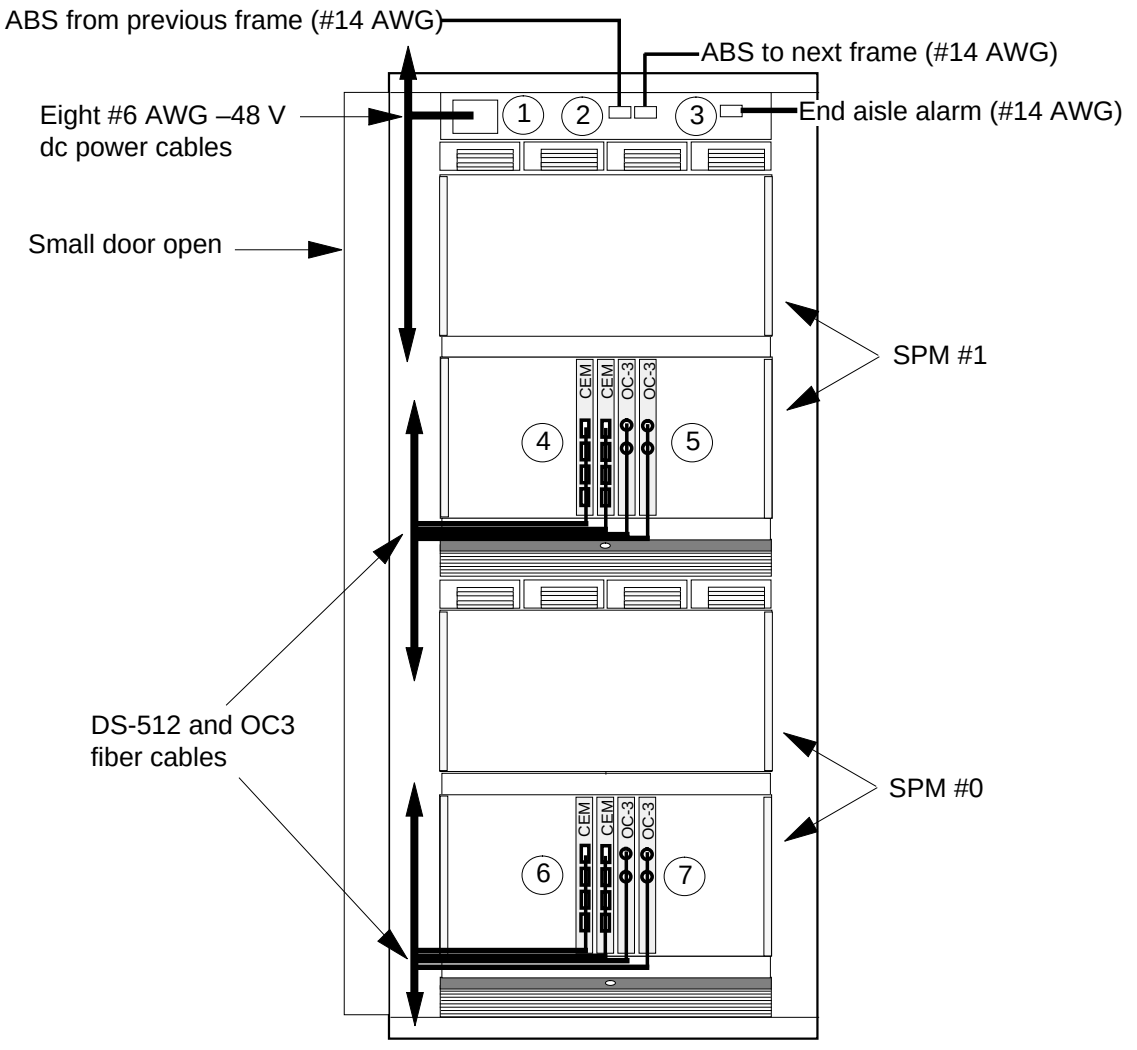
Function	PEC	Number shown in figure	Number of cables	Wire type	Destination
End aisle alarm cable	NT0X96LX	3	1	multiple	End aisle alarm panel (if required)
SPM frame to SPM frame	NT0X96LS	not shown	1	multiple	Next SPM frame (if required)
SPM frame to DTCI frame	NT0X96LQ	not shown	1	multiple	Digital trunk controller ISDN (DTCI) frame (if required)
SPM frame to MSP frame	NT0X96LR	not shown	1	multiple	Modular support panel (MSP) frame
SPM frame to AXU	NT0X96LT	not shown	1	multiple	Alarm cross-connect unit (AXU)
DS-512 from SPM #1	NTLO97AW	4	4	HCS fiber	ENET
OC3 from SPM #1	NTLX81AA	5	4	Fiber adapter kit	Fiber manager
DS-512 from SPM #0	NTLO97AW	6	4	HCS fiber	ENET
OC3 from SPM #0	NTLX81AA	7	4	Fiber adapter kit	Fiber manager

Note: The NTLX81AA Fiber Adapter Kit is shipped loose—one kit for each OC3 module.

Cabling layout

The following figure shows the cabling layout.

NTLX50AA SPM-DMS frame assembly (continued)

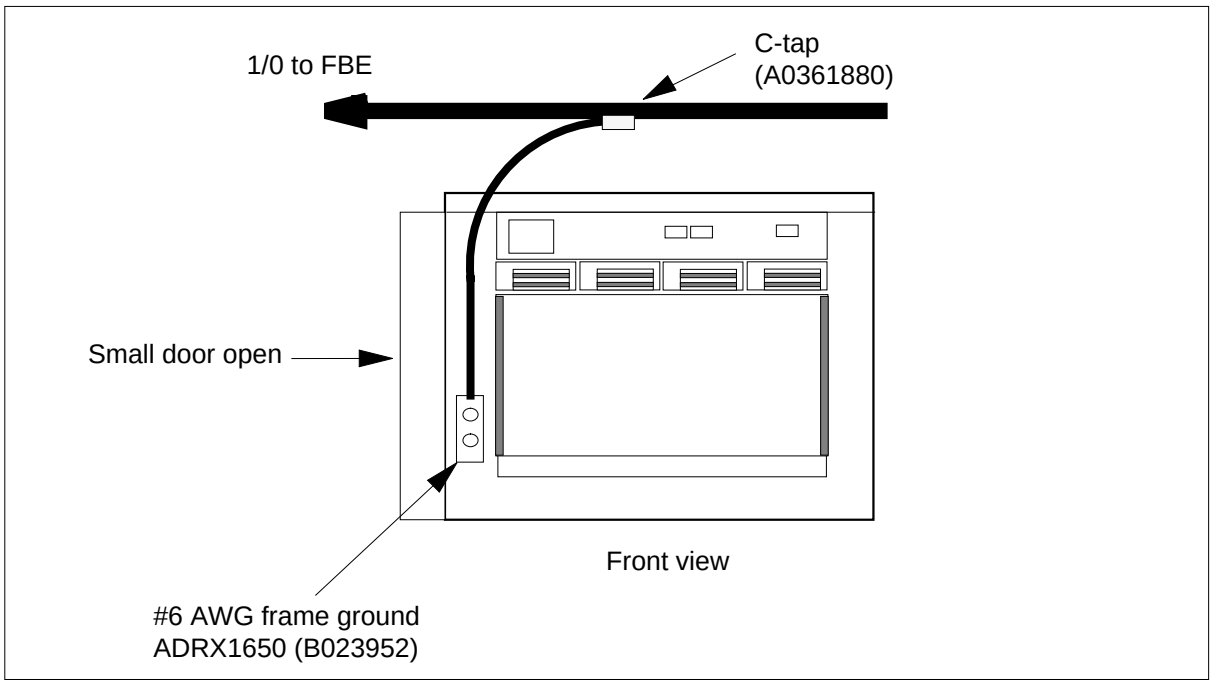


Note: Fiber, alarm, and power cables can be routed up to cable racks or down to the raised floor.

NTLX50AA SPM-DMS frame assembly (continued)

Frame ground

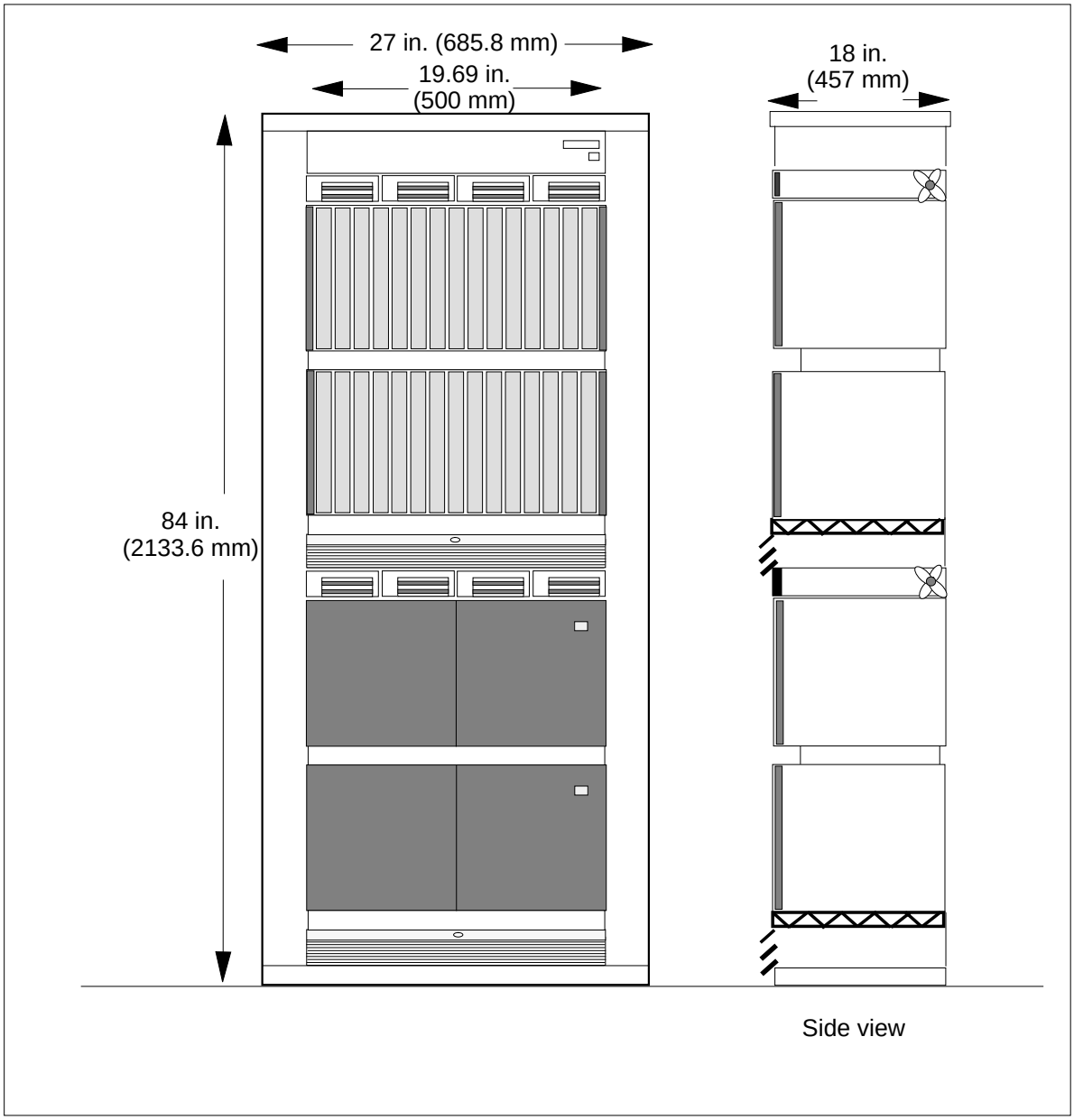
The following figure shows the #6 AWG frame ground connection mounted on the left front of the NTLX50AA frame assembly. The frame ground cable requires a C-tap to a 1/0 cable connected to the frame bonding equalizer (FBE) and routed in the cable trough throughout the length of the frame line up.



Frame design

For the North American market, SPM installs in a DMS frame that measures 7 ft (2133.6 mm) x 2.25 ft (457 mm) x 1.5 ft (457 mm). The following figure shows the NTLX50AA DMS frame dimensions.

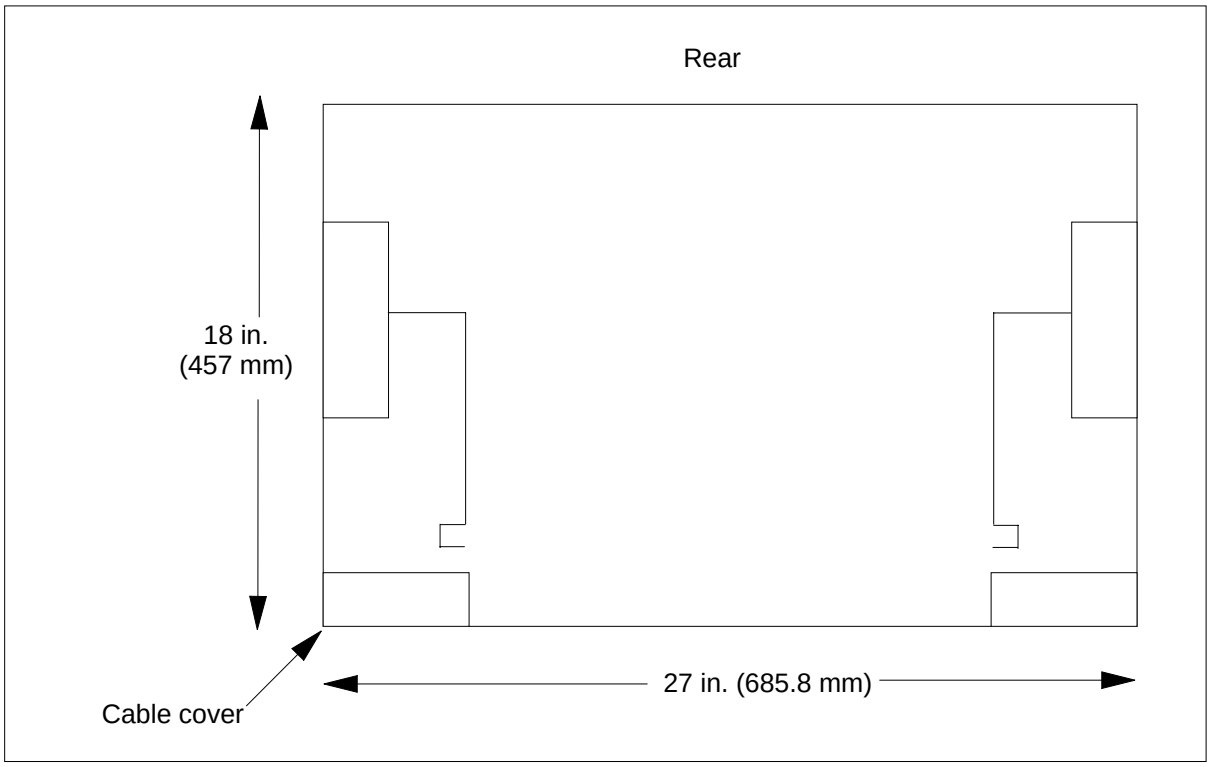
NTLX50AA SPM-DMS frame assembly (continued)



Floor footprint

The following figure shows the footprint of a NTLX50AA DMS frame. The NTLX50AA frame is capable of housing two SPM nodes in this area.

NTLX50AA SPM-DMS frame assembly (end)



NTLX51AA dual-shelf assembly

Description

The NTLX51AA dual-shelf assembly resides in the NTOX25BE gray framework assembly and houses the DMS-Spectrum Peripheral Module (SPM) printed circuit pack (PCP) modules.

Components

The components of the the NTLX51AA dual-shelf assembly are

- NTLX5016 air filter tray assembly (one for each dual-shelf assembly)
- NTLX5101 shelf mechanical assembly (one for each dual-shelf assembly)
- NTLX5201 backplane assembly (one for each dual-shelf assembly)
- NTLX60AA blank filler faceplate (0 to 22 for each dual-shelf assembly)
- NTLX61AA shelf interface module (SIM) (two for each dual-shelf assembly)
- NTLX63AA, NTLX82AA, or NTLX82BA common equipment module (CEM) (two for each dual-shelf assembly)

  Note: The NTLX63AA CEM is not compatible with SP15.

- NTLX65AA or NTLX65BA digital signal processor (DSP) resource module (RM) (0 to 24 DSP RMs for each dual-shelf assembly)
- NTLX66AA or NTLX66BA voice signal processor (VSP) RM (0 to 24 VSP RMs for each dual-shelf assembly)

  Note: Support exists for any combination of up to 24 DSP and VSP RMs. Typically, the number of necessary DSP and VSP RMs will be less than this.

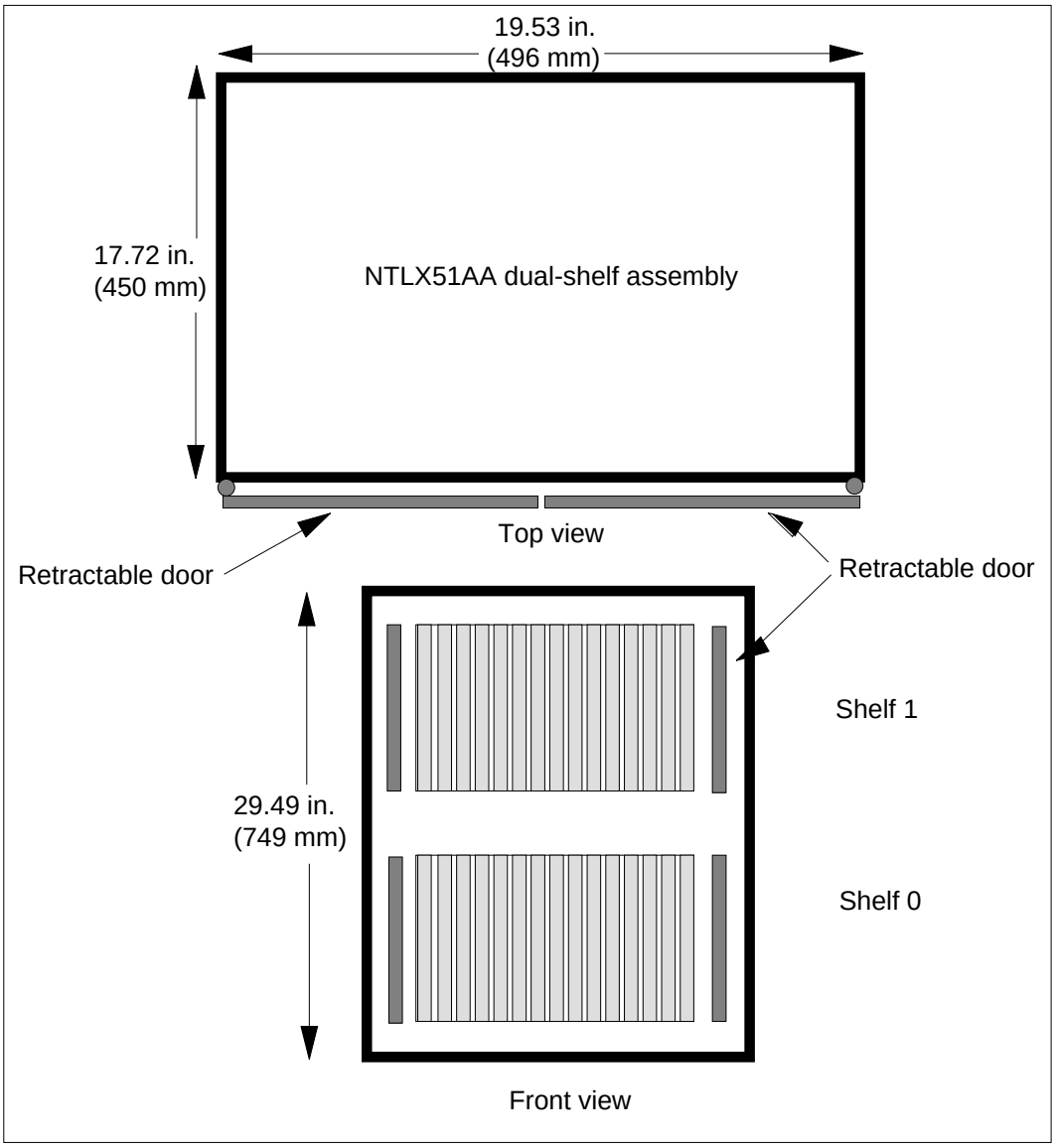
- NTLX71AA or NTLX71BA OC3 interface module (two for each dual-shelf assembly)
- NTLX72AA data link controller (DLC) RM (two for each dual-shelf assembly)

ATTENTION
Not all modules apply to all markets.

NTLX51AA dual-shelf assembly (continued)

Design

As shown in the following figure, the NTLX51AA dual-shelf assembly is 19.53 in. (496 mm) wide, 17.72 in. (450 mm) deep, and 29.49 in. (749 mm) high.



NTLX51AA dual-shelf assembly (continued)

Features

The NTLX51AA dual-shelf assembly features are

- retractable doors for cable protection
- front access of modules and connectors
- 28 module positions plus two power modules all at 1.25 in. (32 mm) pitch
- module keying that provides for 64 key positions
- backplane guide pins for module alignment
- advanced electrostatic discharge (ESD) ground to modules

Backplane

The NTLX51AA dual-shelf assembly has a single NTLX5201 backplane and uses a five-column background connector system with male contacts on the backplane and female contacts on the plug in modules. The NTLX5201 backplane provides an eight-layer single backplane for the NTLX51AA dual-shelf assembly. The NTLX5201 backplane has the following features:

- The assembly is 19.37 in. (492 mm) high and 29.41 in. (747 mm) wide.
- The assembly is a 10-layer printed circuit board.
- The assembly has 30 card slots.
- Slots consist of a one-SU 0.1 in. (2.5 mm) 35-pin Molex connector (used specifically for power and frame ground).
- Slots consist of two-SU 0.1 in. (2.5 mm) 85-pin Molex connector (used specifically for digital signals).
- CEM slots consist of one ten-SU 0.1 in. (2.5 mm) 475-pin Molex connector (used specifically for digital signals).

Module physical characteristics

The physical characteristics that apply to all SPM modules are described in this section. See the individual module descriptions in this manual for specific information on the electronic specifications and performance of each module.

Modules used in the SPM dual-shelf assembly have the following common physical characteristics:

- Each module is 1.22 in. (31 mm) wide, 12.4 in. (315 mm) high, and 15.75 in. (400 mm) deep.
- Modules have a minimum of 60% of the cross-sectional area open for air flow.

- Each module contains a single circuit board that is 12.01 in. (305 mm) high by 14.17 in. (360 mm) deep.
- Modules that require external optical or electical cable connections have cable connectors on the front panel.
- Modules weigh 9 lbs (4 kg) or less.
- Module packaging provides EMI and EMC shielding of 55 db up to 1 GHz.
- Modules can dissipate up to 55 W of power by allowing 150 linear ft/min (7.5 m/s) of air flow through the module.

Module Location

The following figure shows the NTLX51AA dual-shelf assembly module locations with module slot locations.

CAUTION
Air and electro-magnetic interference integrity
Slots that do not contain an RM must have filler modules installed to maintain air and electro-magnetic interference integrity.

The NTLX51AA dual-shelf assembly has a maximum of 30 card slots available for peripheral and system support modules. The NTLX51AA dual-shelf assembly must have the following provisioned modules:

- NTLX61AA SIM A and SIM B located in slot A, at right-hand end of shelf 0 and shelf 1.
- NTLX71AA or NTLX71BA OC3 interface modules located in slots 9 and 10 of shelf 0.
- NTLX63AA, NTLX82AA, or NTLX82BA CEM 0 and CEM 1 located in slots 7 and 8 of shelf 0.

  Note: The NTLX63AA CEM is not compatible with SP15.

- With the remaining 24 slots provisioned according to specific applications.

The NTLX51AA dual-shelf assembly limits the CEM and OC3 interface modules to specific slot locations because of the additional communications resources needed by the modules.

The OC3 interface modules use slots 9 and 10 because of their bandwidth requirements. These slots have six extra links that provide two additional S-link clusters, delivering full-bandwidth-payload termination for OC3.

NTLX51AA dual-shelf assembly (continued)

The recommended position of the DLC RMs is in slots 1 and 7 of shelf 1.

The DSP RMs and VSP RMs are permitted in all slots that are not reserved for system-level modules (SIM, CEM, or OC3 modules).

Note: All modules may not apply to all markets.

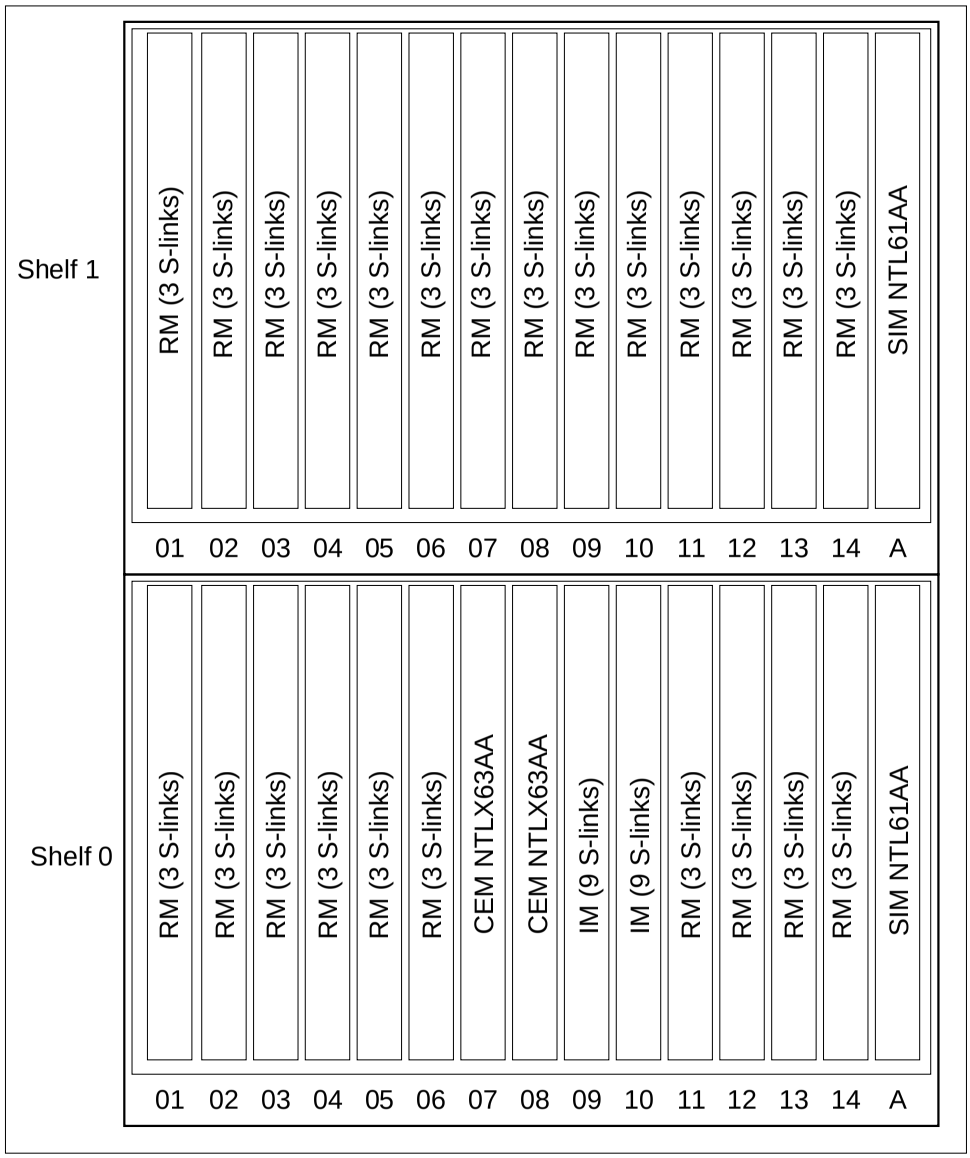
Available S-links

S-links are available to card slots as follows:

- Slots 9 and 10 on the lower shelf each provide 9 S-links
- All other slots each provide 3 S-links

The following figure shows the number of S-links available at the card slot (inside the dual-shelf assembly).

NTLX51AA dual-shelf assembly (continued)



The following table describes the NTLX51AA dual-shelf assembly resource modules, system modules, and the enhanced network (ENET) NT9X40DA paddleboard.

NTLX51AA dual-shelf assembly (continued)

The NT9X40DA paddleboard resides in the ENET and connects to the SPM equipment through fiber-optic interconnects.

PEC	Slot/shelf	Description
NT9X40DA	Resides in ENET	ENET quad DS-512S fiber link interface paddleboard
NTLX61AA	Slot 15/shelf 0, Slot 15/shelf 1	SIM
NTLX63AA, NTLX82AA, NTLX82BA	Slots 7 and 8/shelf 0	CEM
NTLX65AA, NTLX65BA	Slots 9-13/shelf 1	DSP RM
NTLX66AA, NTLX66BA, NTLX85AA, NTLX86AA	Slots 3, 4, and 11-14/shelf 0, Slots 5, 6, and 14/shelf 1	VSP RM
NTLX71AA, NTLX71BA	Slots 9 and 10/shelf 0	OC3 interface module
NTLX72AA	Slots 1 and 7/shelf 1	DLC RM

Note 1: The NTLX63AA CEM is not compatible with SP15.

Note 2: The quantities and locations of DSP and VSP RMs are office dependent.

Note 3: All modules may not apply to all markets.

RM capacities

The actual provisioning for DSP RM and VSP RM is application dependent. The following tables show the islands' capacities for each service used within an application.

ATTENTION
The voice signal processor (VSP) does not apply to all markets.

NTLX51AA dual-shelf assembly (end)

Each DSP RM provides nine DSP islands (DSPI). Each of the nine islands on a DSP RM can be configured for a different application. A single DSPI can provide only one type of service application at any given time.

DSP RM application (function)	Quantity per DSPI
Tone synthesizer (TONESYN)	255
Multi frequency receiver (MF)	40
Continuity tone transceiver (COT)	80
DTMF receiver with dial tone generation	64
AB bit handler (ABBH)	14

Each VSP RM provides 10 turbo DSP islands (tDSPI).

VSP RM application (function)	Quantity per tDSPI
Echo canceller (ECAN)	26

NTLX51BA dual-shelf assembly

Description

The NTLX51BA dual-shelf assembly resides in the NTOX25BE gray framework assembly and houses the DMS-Spectrum Peripheral Module (SPM) printed circuit pack (PCP) modules.The NTLX51BA dual-shelf assembly is a replacement for the NTLX51AA dual-shelf assembly.

The following are the enhancements available when NTLX51AA is upgraded to the NTLX51BA:

- The NTLX51BA dual-shelf assembly provides four high speed slots to accomodate resource modules (RMs) that have high bandwidth needs, while the NTLX51AA dual-shelf assembly only provides two.
- The NTLX51BA provides four low speed slots to accomodate RMs that have low bandwidth needs, while the NTLX51AA provides none.

Components

The components of the the NTLX51BA dual-shelf assembly are

- NTLX5016 air filter tray assembly (one for each dual-shelf assembly)
- NTLX5101 shelf mechanical assembly (one for each dual-shelf assembly)
- NTLX5211 backplane assembly (one for each dual-shelf assembly)
- NTLX60AA blank filler faceplate (0 to 22 for each dual-shelf assembly)
- NTLX61AA shelf interface module (SIM) (two for each dual-shelf assembly)
- NTLX63AA, NTLX82AA, or NTLX82BA common equipment module (CEM) (two for each dual-shelf assembly)

  Note: The NTLX63AA CEM is not compatible with SP15.

- NTLX65AA or NTLX65BA digital signal processor (DSP) resource module (RM) (0 to 24 DSP RMs for each dual-shelf assembly)
- NTLX66AA, NTLX66BA, NTLX85AA, or NTLX86AA voice signal processor (VSP) RM (0 to 24 VSP RMs for each dual-shelf assembly)

  Note: Support exists for any combination of up to 24 DSP and VSP RMs. Typically, the number of necessary DSP and VSP RMs will be less than this.

NTLX51BA dual-shelf assembly (continued)

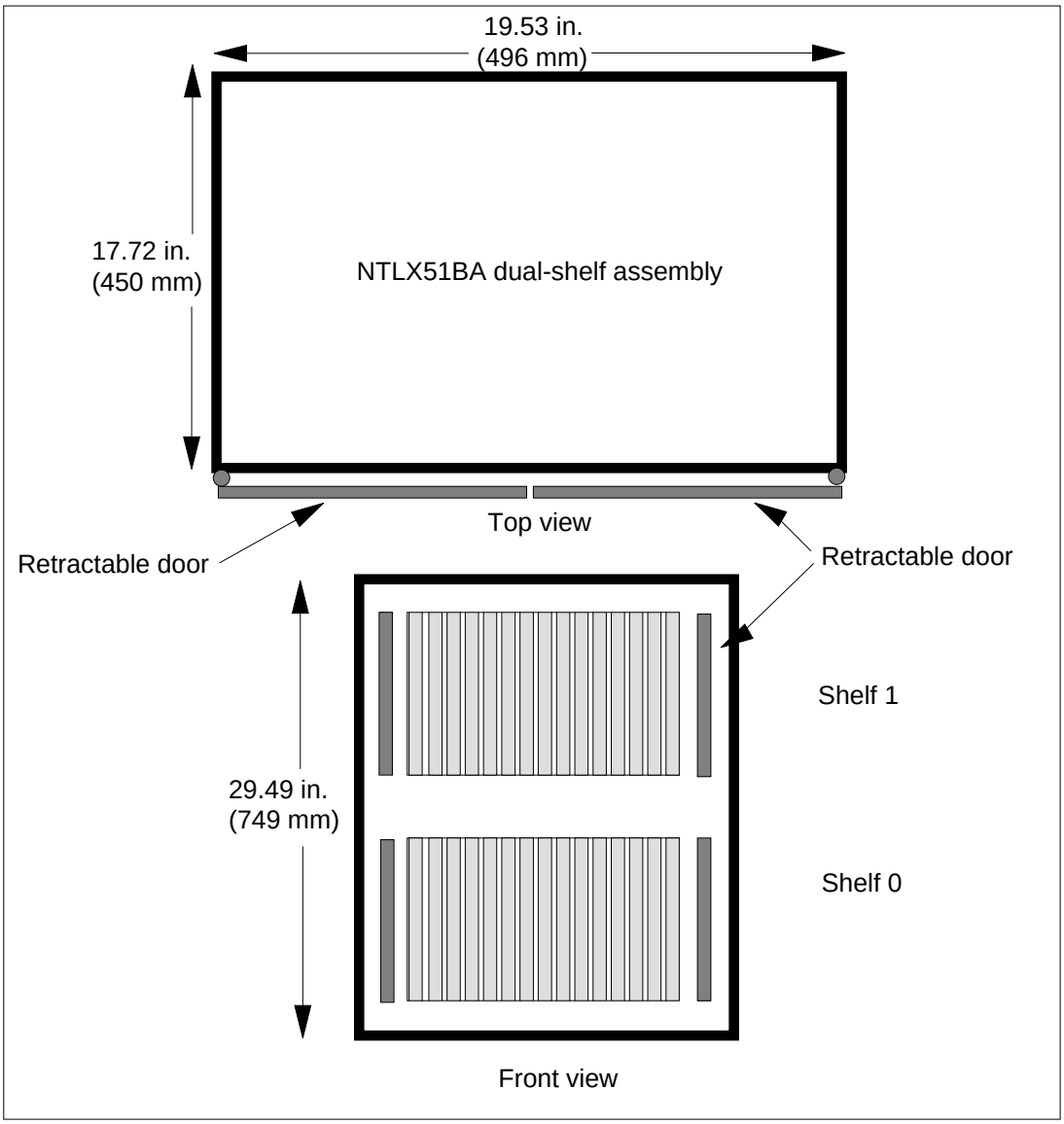
- NTLX71AA or NTLX71BA OC3 interface module (0 or 2 for each dual-shelf assembly)
- NTLX72AA data link controller (DLC) RM (0 or 2 DLC RMs for each dual-shelf assembly)

ATTENTION
Not all modules apply to all markets.

Design

As shown in the following figure, the NTLX51BA dual-shelf assembly is 19.53 in. (496 mm) wide, 17.72 in. (450 mm) deep, and 29.49 in. (749 mm) high.

NTLX51BA dual-shelf assembly (continued)



Features

The NTLX51BA dual-shelf assembly features are

- retractable doors for cable protection
- front access of modules and connectors
- 28 module positions plus two power modules all at 1.25 in. (32 mm) pitch
- module keying that provides for 64 key positions

- backplane guide pins for module alignment
- advanced electrostatic discharge (ESD) ground to modules

Backplane

The NTLX51BA dual-shelf assembly has a single NTLX5211 backplane and uses a five-column background connector system with male contacts on the backplane and female contacts on the plug in modules. The NTLX5211 backplane provides a ten-layer single backplane for the NTLX51BA dual-shelf assembly. The NTLX5211 backplane has the following features:

- The assembly is 19.37 in. (492 mm) high and 29.41 in. (747 mm) wide.
- The assembly is a 10-layer printed circuit board.
- The assembly has 30 card slots.
- Slots consist of a one-SU 0.1 in. (2.5 mm) 35-pin Molex connector (used specifically for power and frame ground).
- Slots consist of two-SU 0.1 in. (2.5 mm) 85-pin Molex connector (used specifically for digital signals).
- CEM slots consist of one ten-SU 0.1 in. (2.5 mm) 475-pin Molex connector (used specifically for digital signals).

Module physical characteristics

The physical characteristics that apply to all SPM modules are described in this section. See the individual module descriptions in this manual for specific information on the electronic specifications and performance of each module.

Modules used in the SPM dual-shelf assembly have the following common physical characteristics:

- Each module is 1.22 in. (31 mm) wide, 12.4 in. (315 mm) high, and 15.75 in. (400 mm) deep.
- Modules have a minimum of 60% of the cross-sectional area open for air flow.
- Each module contains a single circuit board that is 12.01 in. (305 mm) high by 14.17 in. (360 mm) deep.
- Modules that require external optical or electical cable connections have cable connectors on the front panel.
- Modules weigh 9 lbs (4 kg) or less.
- Module packaging provides EMI and EMC shielding of 55 db up to 1 GHz.
- Modules can dissipate up to 55 W of power by allowing 150 linear ft/min (7.5 m/s) of air flow through the module.

NTLX51BA dual-shelf assembly (continued)

Module Location

The following figure shows the NTLX51BA dual-shelf assembly module locations with module slot locations.

CAUTION
Air and electro-magnetic interference integrity
Slots that do not contain an RM must have filler modules installed to maintain air and electro-magnetic interference integrity.

The NTLX51BA dual-shelf assembly has a maximum of 30 card slots available for peripheral and system support modules. The NTLX51BA dual-shelf assembly must have the following provisioned modules:

- NTLX61AA SIM A and SIM B located in slot A, at right-hand end of shelf 0 and shelf 1.
- NTLX71AA or NTLX71BA OC3 interface modules located in slots 9 and 10 of shelf 0.
- NTLX63AA, NTLX82AA, or NTLX82BA CEM 0 and CEM 1 located in slots 7 and 8 of shelf 0.

  Note: The NTLX63AA CEM is not compatible with SP15.

- With the remaining 24 slots provisioned according to specific applications.

The NTLX51BA dual-shelf assembly limits the CEM and the OC3 interface modules to specific slot locations because of the additional communications resources needed by the modules.

A pair of OC3 interface modules (one active and one spare) uses slots 9 and 10 of shelf 0 because of bandwidth requirements. These high-speed slots have additional bandwidth to satisfy the bandwidth requirements of the OC3.

The recommended position of the DLC RMs is in slots 1 and 7 of shelf 1.

The DSP RMs and VSP RMs are permitted in all slots that are not reserved for system-level modules (SIM, CEM, and OC3).

Note: All modules may not apply to all markets.

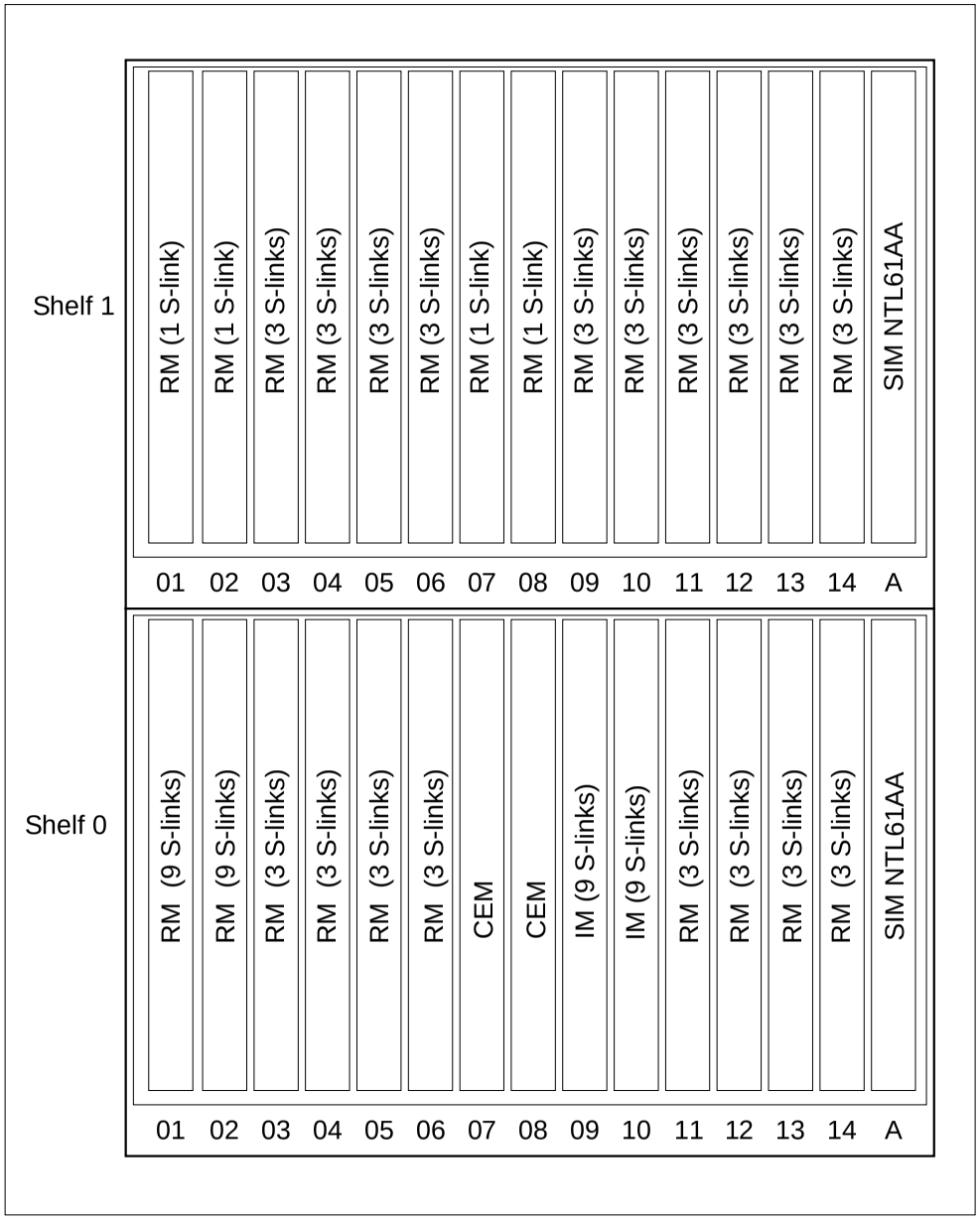
Available S-links

S-links are available to card slots as follows:

- Slots 1, 2, 7, and 8 on the upper shelf each provide 1 S-link
- Slots 1, 2, 9 and 10 on the lower shelf each provide 9 S-links
- All other slots each provide 3 S-links

The following figure shows the number of S-links available at each card slot inside the high speed dual-shelf assembly.

NTLX51BA dual-shelf assembly (continued)



The following table describes the NTLX51BA dual-shelf assembly resource modules, system modules, and the enhanced network (ENET) NT9X40DA paddleboard.

NTLX51BA dual-shelf assembly (continued)

The NT9X40DA paddleboard resides in the ENET and connects to the SPM equipment through fiber-optic interconnects.

PEC	Slot/shelf	Description
NT9X40DA	Resides in ENET	ENET quad DS-512S fiber link interface paddleboard
NTLX61AA	Slot 15/shelf 0, Slot 15/shelf 1	SIM
NTLX63AA, NTLX82AA, NTLX82BA	Slots 7 and 8/shelf 0	CEM
NTLX65AA, NTLX65BA	Slots 9-13/shelf 1	DSP RM
NTLX66AA, NTLX66BA, NTLX85AA, NTLX86AA	Slots 3, 4, and 11-14/shelf 0, Slots 5, 6, and 14/shelf 1	VSP RM
NTLX71AA, NTLX71BA	Slots 9 and 10/shelf 0	OC3 interface module
NTLX72AA	Slots 1 and 7/shelf 1	DLC RM

Note 1: The NTLX63AA CEM is not compatible with SP15.

Note 2: The quantities and locations of DSP and VSP RMs are office dependent.

Note 3: All modules may not apply to all markets.

RM capacities

The actual provisioning for DSP RM and VSP RM is application dependent. The following tables show the islands' capacities for each service used within an application.

ATTENTION
The voice signal processor (VSP) does not apply to all markets.

NTLX51BA dual-shelf assembly (end)

Each DSP RM provides nine DSP islands (DSPI). Each of the nine islands on a DSP RM can be configured for a different application. A single DSPI can provide only one type of service application at any given time.

DSP RM application (function)	Quantity per DSPI
Tone synthesizer (TONESYN)	255
Multi frequency receiver (MF)	40
Continuity tone transceiver (COT)	80
DTMF receiver with dial tone generation	64
AB bit handler (ABBH)	14

Each VSP RM provides 10 turbo DSP islands (tDSPI).

VSP RM application (function)	Quantity per tDSPI
Echo canceller (ECAN)	26

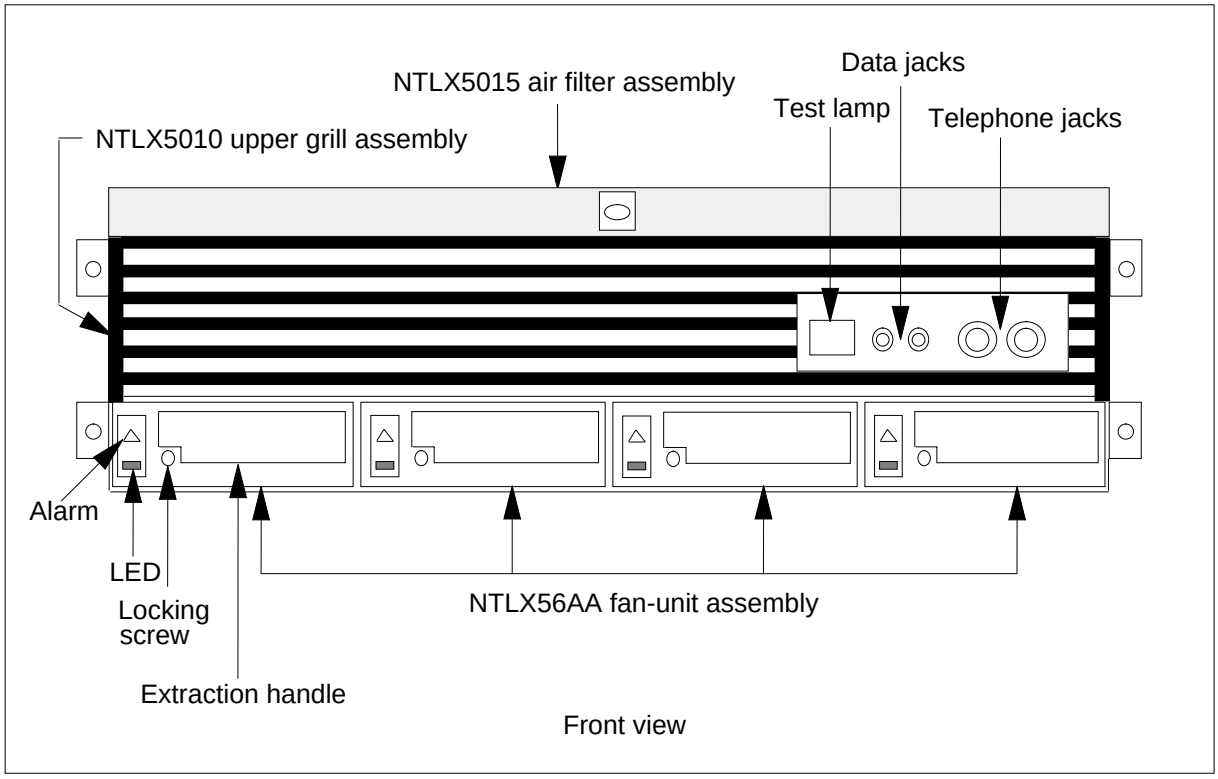
NTLX55AA cooling unit and grill assemblies

Description

The DMS-Spectrum Peripheral Module (SPM) NTLX55AA cooling unit provides

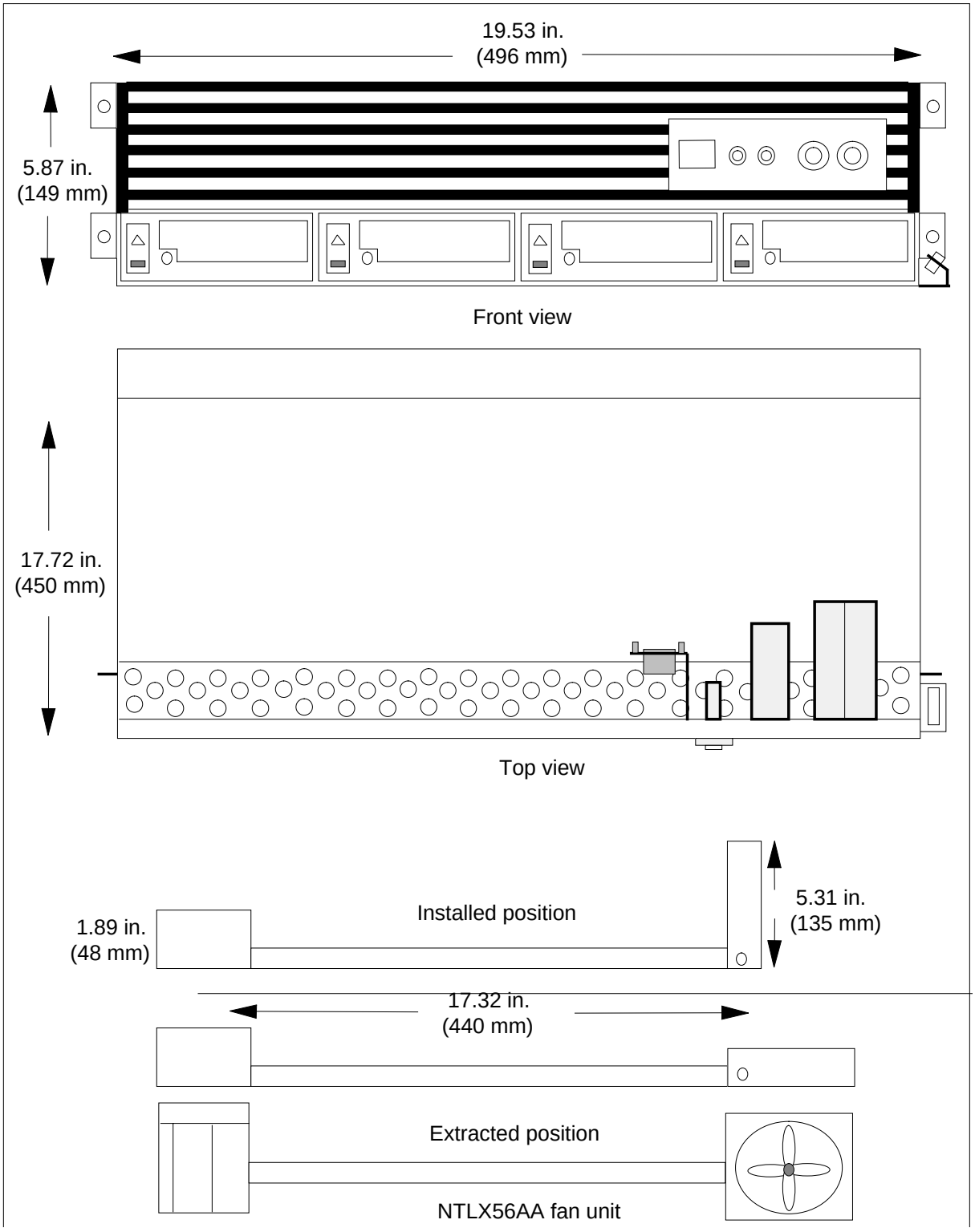
- the basic sheet metal mounts for four NTLX56AA fan units and a grill assembly
- the necessary support electronics for operation and alarms

One NTLX55AA cooling unit is required for each NTLX51AA or NTLX51BA dual-shelf assembly. The following figure shows the NTLX55AA cooling unit, its location, the NTLX5010 upper grill assembly, and an NTLX5015 air filter assembly.



As shown in the following figure, the NTLX55AA cooling unit and NTLX5110 upper grill assembly is 19.53 in. (496 mm) wide, 5.87 in. (149 mm) high, and 17.72 in. (450 mm) deep.

NTLX55AA cooling unit and grill assemblies (continued)



NTLX55AA cooling unit and grill assemblies (continued)

Components

Cooling unit

The cooling unit provides

- four replaceable NTLX56AA fan units
- a baffle for airflow management
- front access to the fan units
- fan power-termination and alarm interfaces
- sufficient airflow to maintain cooling effectiveness if a single fan fails

Cooling air filtration

As shown in the following figure, the NTLX5015 filter assembly rests horizontally at the bottom of each NTLX51AA or NTLX51BA dual-shelf assembly. The foam air filter elements contained in the NTLX5015 assembly are not reusable. Replace the filter periodically, depending on the local dust conditions. The foam filter-element part number is A0665487.

Grill assemblies

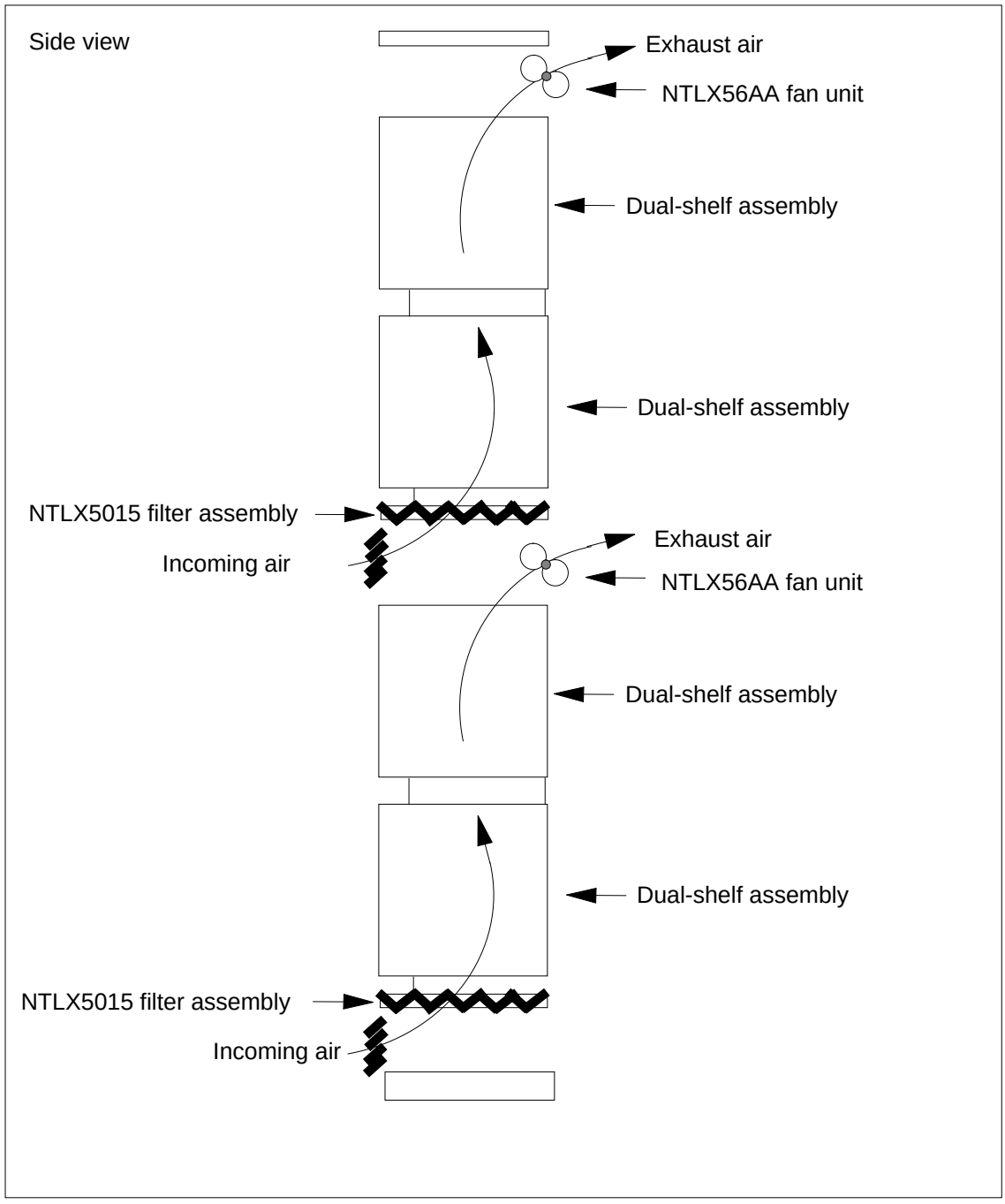
Grill assemblies protect the ambient air intakes that cool the dual-shelf assembly. As shown in the following figure, the bottom dual-shelf assembly draws air through the NTLX5011 lower grill assembly mounted in the bottom of the frame. The upper dual-shelf assembly draws cooling air through the NTLX5010 upper grill assembly located between the dual-shelf assemblies.

The fans draw air through the grills, into the NTLX5015 air filter assemblies, and then into the actual shelves for cooling. The fans expel the air to the rear of the frame assembly.

Fan unit

The NTLX56AA fan units are individually replaceable fans that include mounting slides and connectors. The NTLX56AA fan units are removed by turning the plastic screw clockwise (located on the extraction handle) and pulling the unit out of the NTLX55AA cooling assembly.

NTLX55AA cooling unit and grill assemblies (end)



NTLX57AA PCIU

Description

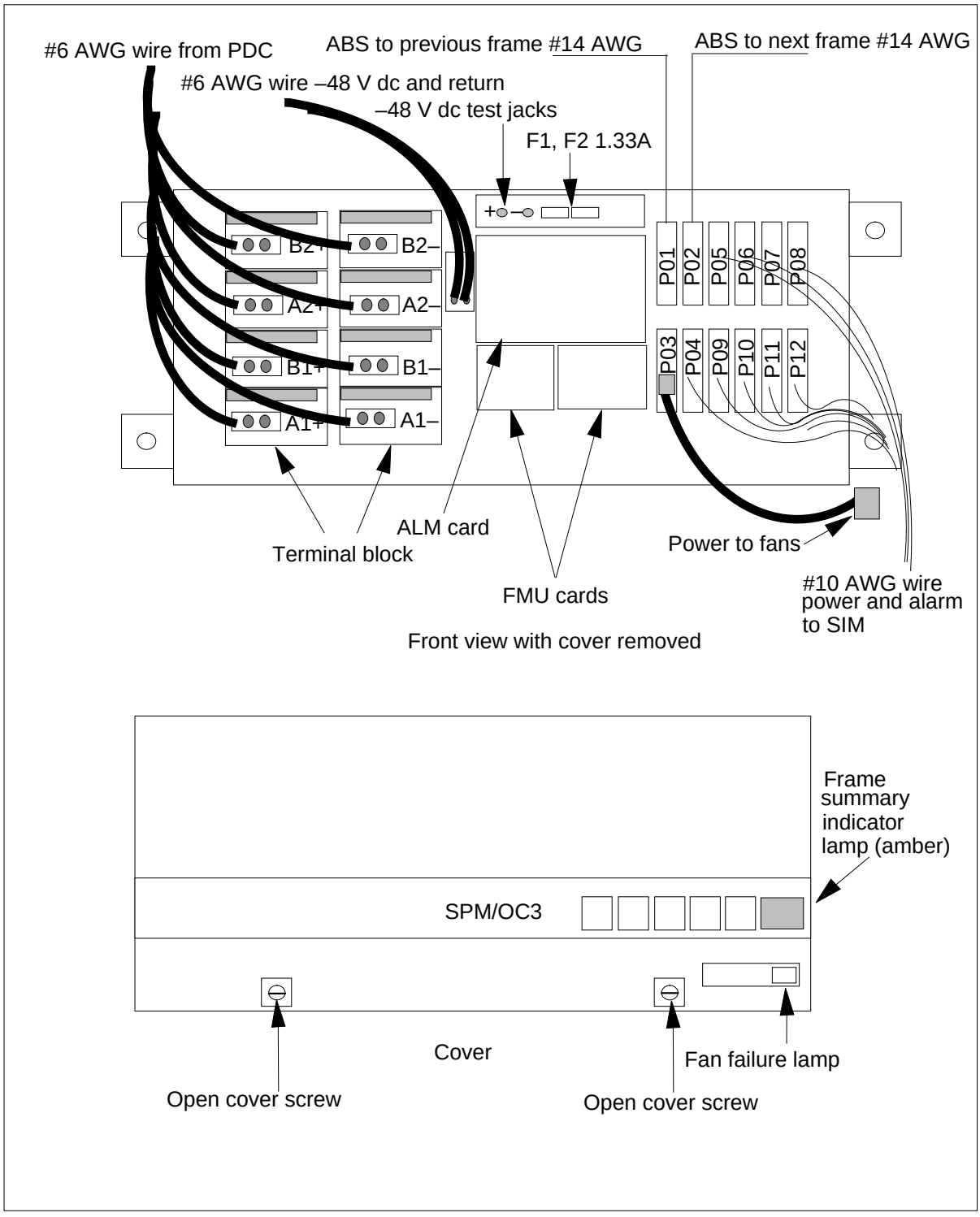
The NTLX57AA power cabling interface unit (PCIU), shown in the following figure, is located in a frame power distribution tray and mounted at the top of the NTOX25BE gray framework assembly. It serves as a central distribution and gathering point for all power and alarm cabling used within the framework assembly of the DMS-Spectrum Peripheral Module (SPM). The NTLX57AA PCIU provides a connection point for the #6 AWG power feed cables from the power distribution center and power and alarm cables, #10 AWG wires, to the NTLX61AA shelf interface modules (SIM) and NTLX55AA cooling units. The NTLX57AA PCIU contains a NTLX58AA alarm card assembly (ALM) and two NTLX59AA fan management units (FMU). A #14 AWG wire from the previous framework assembly with alarm battery supply (ABS) is terminated at P01 (see the following illustration) and sent to the next framework assembly through a #14 AWG wire from P02.

When the frame summary indicator (amber lamp) located on the front cover is off, there are no active alarm in the frame. When the amber lamp is on, there is an active alarm in the frame.

The NTLX57AA PCIU provides the following:

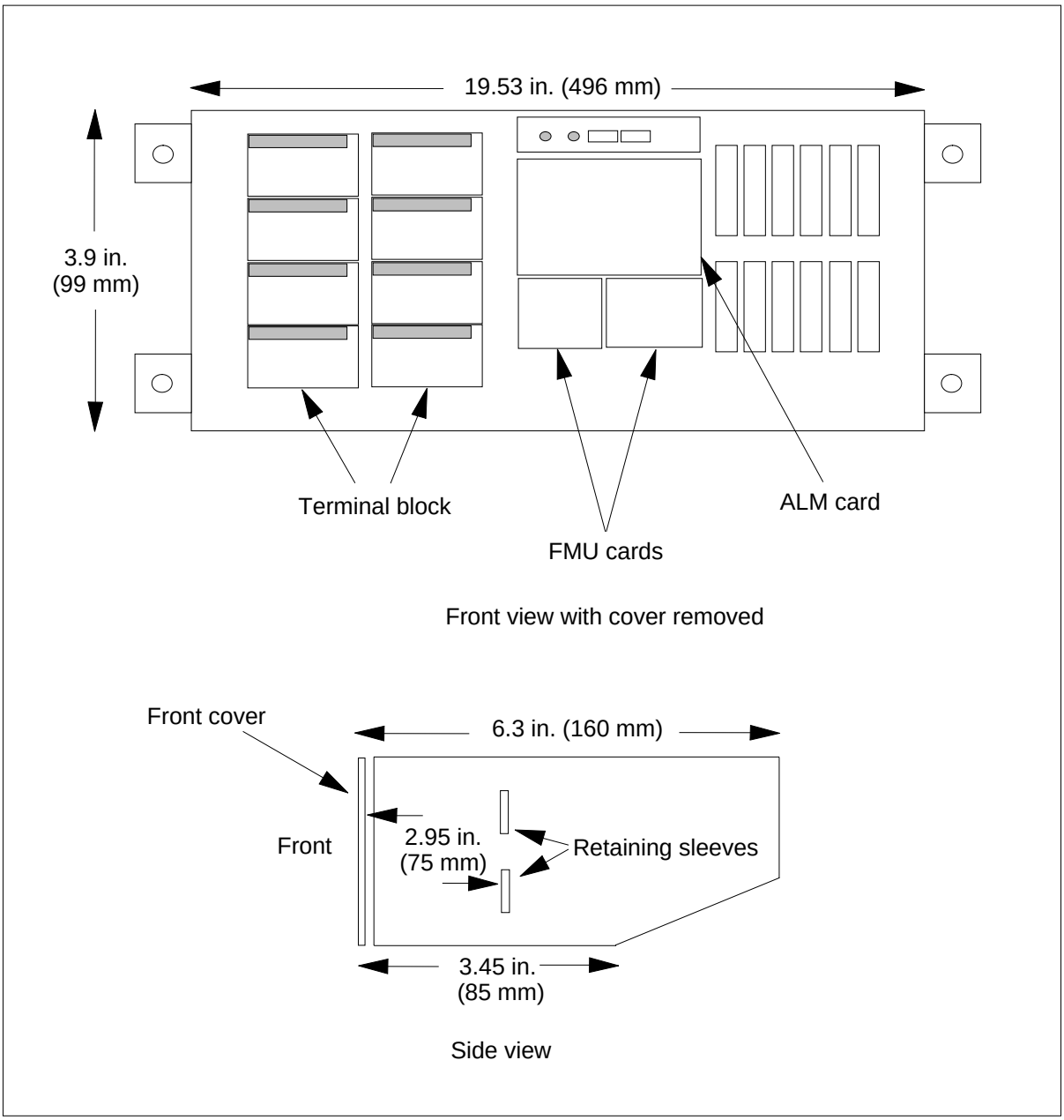
- accommodates up to eight #6 AWG power cables from power distribution center (PDC) and return A (-48 V dc) and B feeds (-48 V dc return)
- accommodates up to sixteen #10 AWG power cables for termination to shelf supply and return A and B feeds
- provides ABS for telephone/data jacks, frame fail LED, and end of aisle LED termination
- provides alarm links to each NTLX51AA or NTLX51BA dual-shelf assembly
- provides -48V dc power (A and B feed) to each NTLX55AA cooling unit
- allows front access to all connections for installation and maintenance

NTLX57AA PCIU (continued)



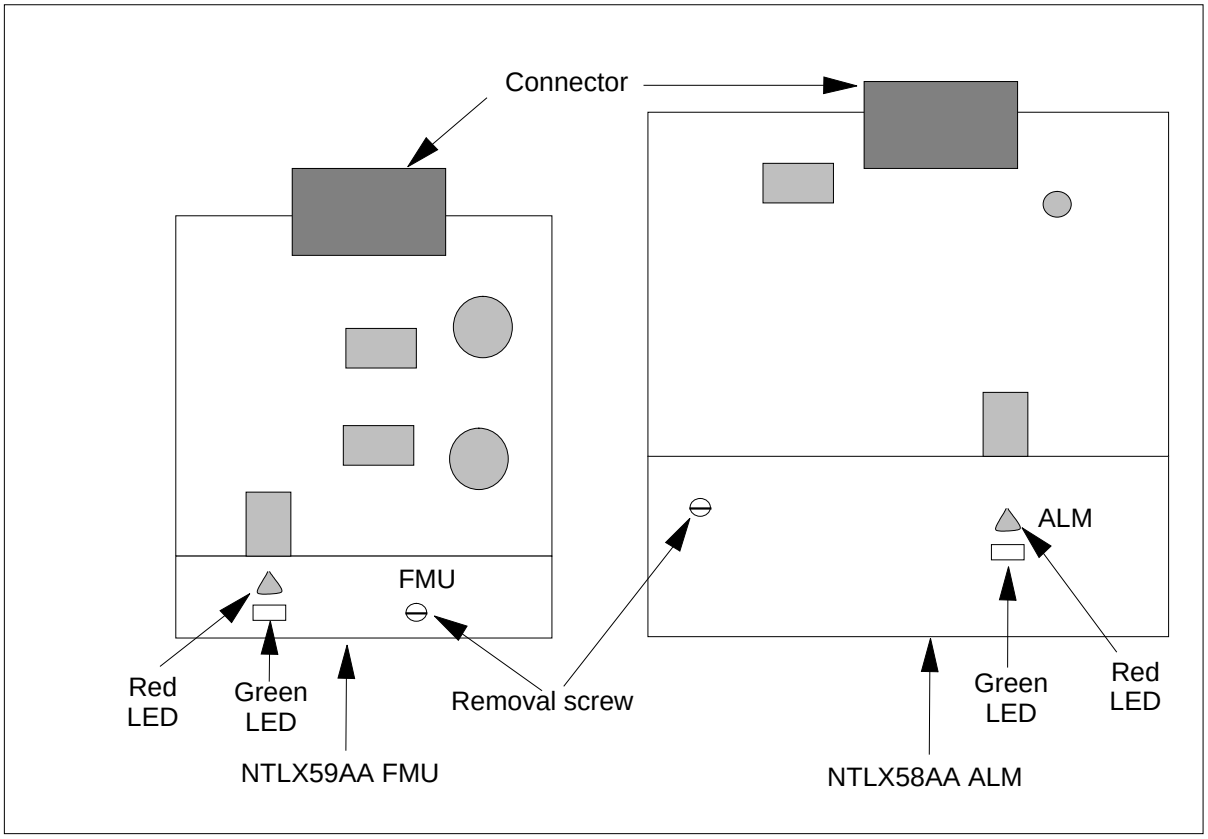
NTLX57AA PCIU (continued)

As shown in the following figure, the NTLX57AA PCIU is 19.53 in. (496 mm) wide, 3.9 in. (99 mm) high, and 6.3 in. (160 mm) deep. The retaining sleeves are 2.95 in. (75 mm) from the front of the NTLX57AA PCIU.



The following figure shows the NTLX58AA ALM and NTLX59AA FMU (PCIU contains two FMUs), which are located in the NTLX57AA PCIU. These three subassemblies are field replaceable components.

NTLX57AA PCIU (continued)



NTLX58AA ALM module functions

The following are the main functions of the NTLX58AA ALM module:

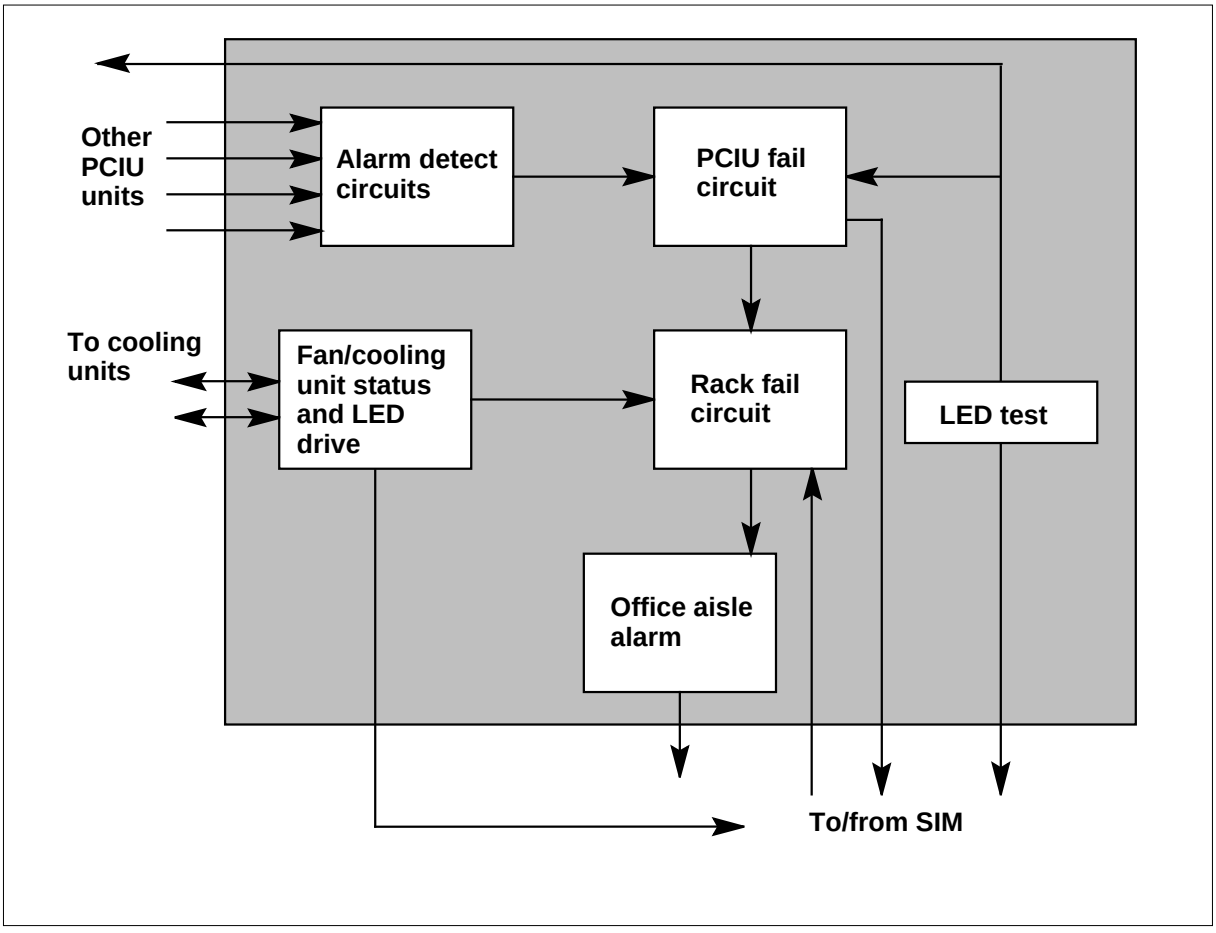
- monitor a maximum of four SIMs
- monitor a maximum of two fan filters
- monitor a maximum of two NTLX55AA cooling units
- provide control for all the fan LEDs
- monitor ABS fuse failures
- report alarms on all NTLX51AA or NTLX51BA dual-shelf assemblies
- report rack failure and PCIU failure indications
- forward major alarm reports to the office alarm unit

ALM module functional blocks

NTLX58AA ALM module has the following functional blocks:

- alarm detection circuits
- PCIU fail circuit
- fan/cooling unit status and LED drive
- rack fail circuit
- LED test
- office aisle alarm

The following figure shows the NTLX58AA ALM module functional block diagram.



NTLX57AA PCIU (continued)

Alarm detection

The alarm detection function accepts alarms from other NTLX57AA PCIUs and the LED test function. It forwards the composite alarm to the PCIU fail circuitry and to the PCIU shelf for further processing.

PCIU fail circuit

The rack fail function combines the PCIU fail signals with the fan/cooling unit status input. The composite signal is applied to the office aisle alarm block for delivery to the row-end alarm display and to the office alarm device.

Fan/cooling unit status and LED drive

Eight fan/cooling unit status and alarms are combined by this function and forwarded to the shelf and to the rack fail circuitry for further processing.

Rack fail circuit

The rack fail circuitry accepts alarm signals from the PCIU fail circuit, the fan/cooling unit status and LED drive function, and from a shelf-level alarm signal. The rack fail circuitry provides alarm input to the office aisle alarm circuitry.

LED test

The LED test function lights the LEDs. It also provides a signal to the dual-shelf assembly that indicates that the LEDs are being tested.

Office aisle alarm

Rack fail and PCIU fail indicators are also driven automatically for PCIU failures or when requested by the shelf. There are two external visual indicators driven by the alarm module: the rack fail LEDs and the PCIU fail LEDs. In addition, the alarm module generates a 10-second (approximate) LED TEST signal when it is activated by a momentary-contact external switch.

Signaling for the NTLX58AA ALM module

The following table shows the signaling and functioning for the NTLX58AA ALM module.

(Sheet 1 of 3)

Pin number	Signal	Function	Comments
2A	BIPFAIL	output	OC (-48/-60 V dc) --> 0 V dc on alarm
2B	AISALM2	output	AISNO --> AISALM1 on alarm
2C	AISALM1	output	AISNO --> AISALM2 on alarm

NTLX57AA PCIU (continued)

(Sheet 2 of 3)

Pin number	Signal	Function	Comments
2D	L+(ABS)	input	0 V dc (1.33 A max)
2E	L+(ABS)	input	0 V dc (1.33 A max)
3C	AISNO	output	AISALM1 --> AISALM2 on alarm
3D	FLTALM1	input	0 V dc --> OC (18V dc) on alarm
3E	FLTALM2	input	0 V dc --> OC (18V dc) on alarm
4C	LEDTEST	input	-48/-60 V dc --> 0 V dc on TEST
4D	CUFAIL2	output	0 V dc --> OC (18 V dc) on alarm
4E	CUFAIL2	output	0 V dc --> OC (18 V dc) on alarm
5B	FOLLOWLED4	input	0 V dc --> OC (18 V dc) on alarm
5C	FOLLOWLED3	input	0 V dc --> OC (18 V dc) on alarm
5D	FOLLOWLED2	input	0 V dc --> OC (18 V dc) on alarm
5E	FOLLOWLED1	input	0 V dc --> OC (18 V dc) on alarm
6D	FOLLOWLED	output	OC (-48/-60 V dc) --> 0 V dc on alarm
6E	BIPLED	output	OC (-48/-60 V dc) --> 0 V dc on alarm
7D	FAN7FAIL	input	0 V dc --> OC (18 V dc) on alarm
7E	FAN8FAIL	input	0 V dc --> OC (18 V dc) on alarm
8D	FAN5FAIL	input	0 V dc --> OC (18 V dc) on alarm
8E	FAN6FAIL	input	0 V dc --> OC (18 V dc) on alarm
9D	FAN3FAIL	input	0 V dc --> OC (18 V dc) on alarm
9E	FAN4FAIL	input	0 V dc --> OC (18 V dc) on alarm
10D	GRNLED8	output	0 V dc --> OC (-48/-60 V dc) on alarm
10E	REDLED8	output	OC (-48/-60 V dc) --> 0 V dc on alarm
11D	GRNLED7	output	0 V dc --> OC (-48/-60 V dc) on alarm
11E	REDLED7	output	OC (-48/-60 V dc) --> 0 V dc on alarm

NTLX57AA PCIU (continued)

(Sheet 3 of 3)

Pin number	Signal	Function	Comments
12D	GRNLED6	output	0 V dc --> OC (-48/-60 V dc) on alarm
12E	REDLED6	output	OC (-48/-60 V dc) --> 0 V dc on alarm
13D	GRNLED5	output	0 V dc --> OC (-48/-60 V dc) on alarm
13E	REDLED5	output	OC (-48/-60 V dc) --> 0 V dc on alarm
14D	GRNLED4	output	0 V dc --> OC (-48/-60 V dc) on alarm
14E	REDLED4	output	OC (-48/-60 V dc) --> 0 V dc on alarm
15D	GRNLED3	output	0 V dc --> OC (-48/-60 V dc) on alarm
15E	REDLED3	output	OC (-48/-60 V dc) --> 0 V dc on alarm
16D	GRNLED2	output	0 V dc --> OC (-48/-60 V dc) on alarm
16E	REDLED2	output	OC (-48/-60 V dc) --> 0 V dc on alarm
17A	FAN2FAIL	input	0 V dc --> OC (18 V dc) on alarm
17B	LEDTSTC	input	10 Uf cap to 0 V dc (LEDTSTNO-->LEDTSTNC to initiate test)
17C	LEDTSTNC	input	750K + 250K to bias FET
17D	GRNLED1	output	0 V dc --> OC (-48/-60 V dc) on alarm
17E	REDLED1	output	OC (-48/-60 V dc) --> 0 V dc on alarm
18A	FAN1FAIL	input	0 V dc --> OC (18 V dc) on alarm
18B	LEDTSTNO	input	-48/-60 V dc (100K)
18C	FUSEALM	input	OC --> -48/-60 V dc on alarm
18D	L-(ABS)	input	-48/-60 V dc (1.33 A max)
18E	L-(ABS)	input	-48/-60 V dc (1.33 A max)

NTLX59AA FMU description

The NTLX59AA FMU provides over-current protection and conducted noise filtering. A soft-start circuit prevents high filter-capacitor in-rush current.

FMU module functions

The main functions of the NTLX59AA FMU are

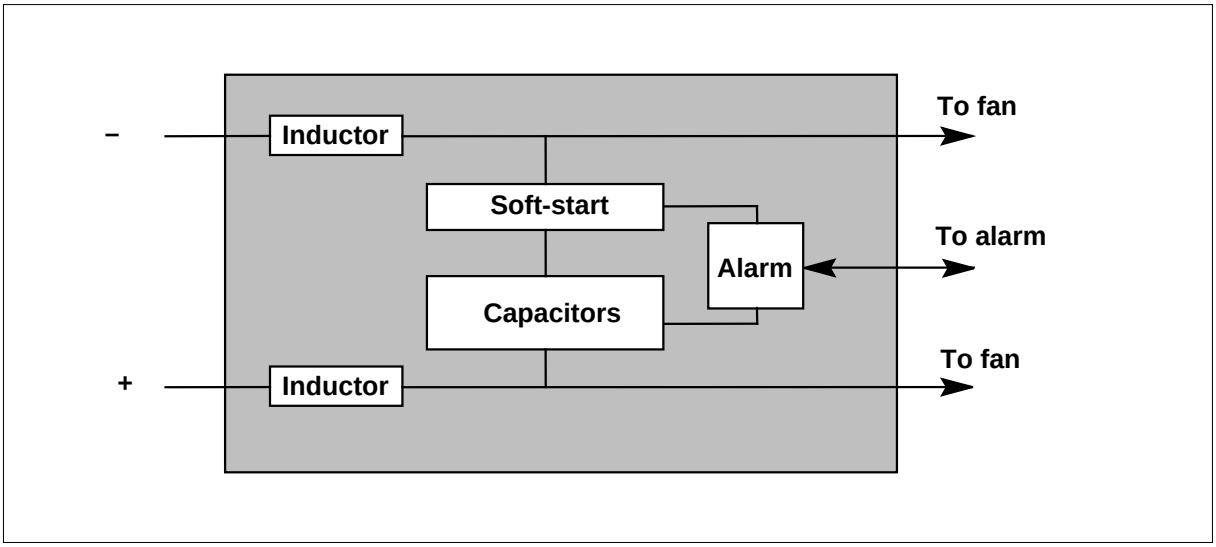
- soft-start—to limit capacitor in-rush current
- capacitor fault alarm
- -48/-60 V at 30 A input capability
- input transient protection

FMU functional blocks

The NTLX59AA FMU has the following functional blocks:

- inductor
- soft-start
- alarm
- capacitors

The following figure shows the block diagram of the NTLX59AA FMU.



Inductor

The inductors are part of the circuit that limits the noise conducted from the fans to the main power bus.

NTLX57AA PCIU (end)

Soft-start

When power is applied, the charging circuit allows the capacitors to charge slowly until they are fully charged. If the capacitor current is excessive, the fuse interrupts the flow of current.

Alarm

The alarm circuitry is triggered by the failure of the capacitor filter or the loss of input power.

Capacitors

The capacitors are part of the circuit that limits the noise conducted from the fans to the main power bus.

Signaling for the NTLX59AA FMU

The following table shows the signaling and pinouts for the NTLX59AA FMU.

Pin number	Signal	Comments
2A-7E	L-	-48/-60 V dc (30 A max)
8A-8E	L-FAN1	-48/-60 V dc (1 A max)
9A-9E	L-FAN2	-48/-60 V dc (1 A max)
12E	LEDTEST	-48/-60 V dc --> 0 V dc on test
13E	FMUALM	0 V dc -->OC on alarm
14A-14E	L+FAN1	0 V dc (1 A max)
15A-15E	L+FAN2	0 V dc (1 A max)
16A-18E	L+	0 V dc (30 A max)

NTLX60AA filler module

Description

The NTLX60AA is an empty module container used in the DMS-Spectrum Peripheral Module (SPM). The NTLX60AA is a filler module that occupies any slot in the NTLX51AA or NTLX51BA shelf assembly that does not contain a resource module. The NTLX60AA must fill any open slots in an active shelf assembly that contains a shelf interface module (SIM). The following caution message appears in provisioning and module-replacement instructions.

CAUTION

Equipment damage due to empty slots

All unused slots on a powered shelf must be equipped with NTLX60AA filler modules. Filler modules maintain electromagnetic interference (EMI) integrity and they maintain shelf airflow patterns to ensure proper cooling.

Location

The NTLX60AA occupies any module slot not occupied by a resource module.

Functional description

The NTLX60AA ensures EMI integrity and cooling-air flow control.

Functional blocks

The NTLX60AA has no functional blocks.

Signaling

The NTLX60AA has no signaling capability.

Pin outs

The NTLX60AA has no connector pins.

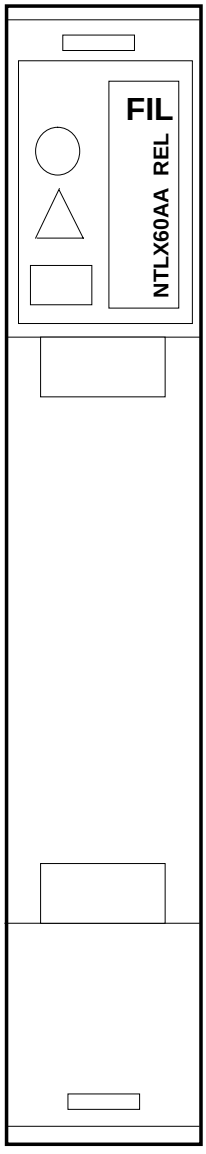
Timing

The NTLX60AA has no timing functionality.

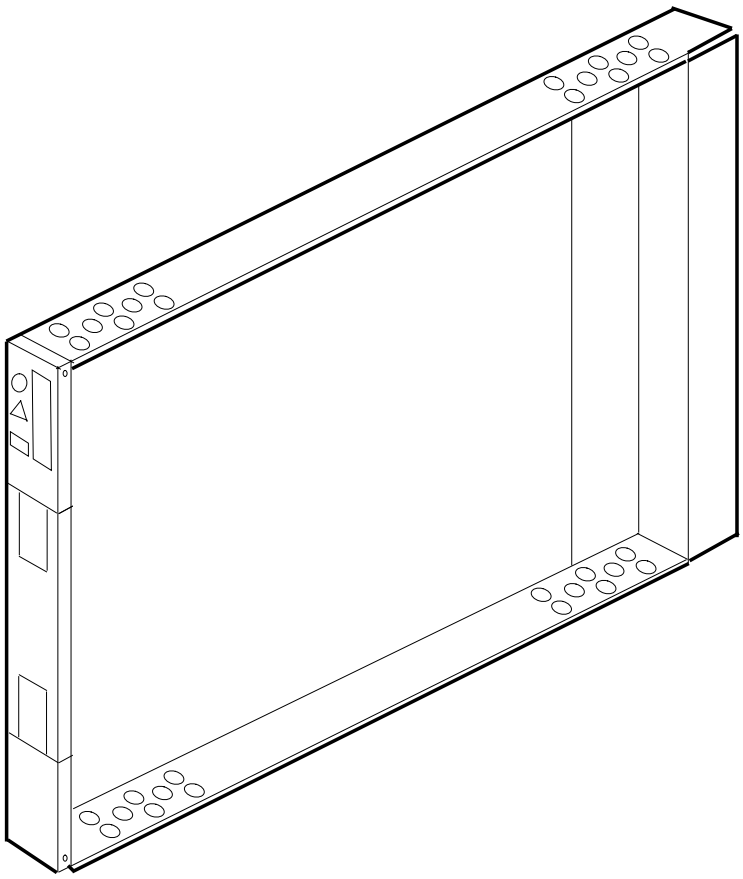
Technical data

The following figure shows the NTLX60AA filler module.

NTLX60AA filler module (end)



Faceplate view



Side view

Power requirements

The NTLX60AA has no power requirements.

NTLX61AA SIM

Description

The NTLX61AA shelf interface module (SIM) is the DC power conditioner for the NTLX51AA or NTLX51BA dual-shelf assembly for the DMS-Spectrum Peripheral Module (SPM). The DC portion of the SIM contains 30 amp dc filters, power switching, and electromagnetic interference (EMI) conditioning.

The slow charge circuitry protects the power conditioning circuit from high-inrush startup conditions.

The NTLX61AA SIM is also the alarm interface between the CEM and the NTLX57AA power connection interface unit (PCIU). The SIM also provides SPM test bus access.

Location

There are two NTLX61AA SIMs in each dual-shelf assembly. One SIM occupies slot A on shelf 0, and the other SIM is located in slot A on shelf 1.

Functions

The NTLX61AA SIM has the following functions:

- current limiting during start up
- filter fail alarm
- power loss alarm
- switch off alarm
- filtered -48/-60 volt at 30 amperes
- power conditioning
- CEM / PCIU alarm interface
- card presence logic
- test bus access

Functional blocks

The NTLX61AA SIM can be functionally divided into the following blocks:

- 30 amp switch
- EMI filter
- soft start circuitry

NTLX61AA SIM (continued)

- dc filter
- alarms and LED drivers

30 amp switch

The 30-ampere switch connects the EMI filters to the power input bus.

EMI filter

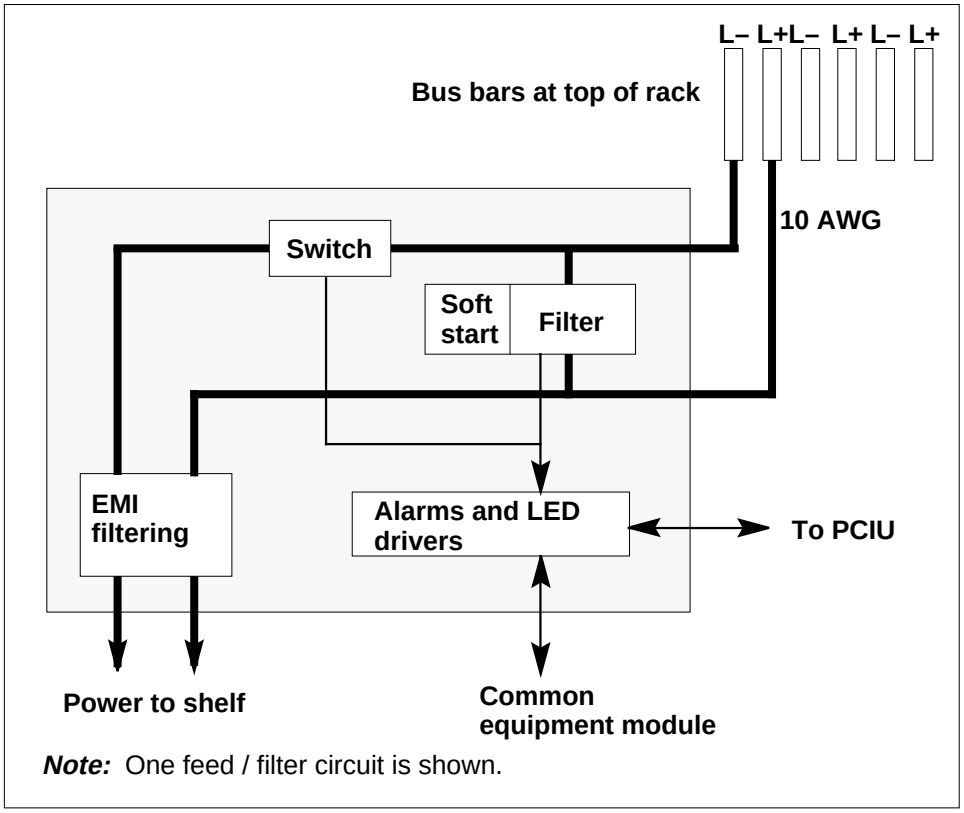
The EMI filter provides filtration of conducted interference to maintain FCC/CSA-mandated standards.

Alarms and LED drivers

The alarms and LED drivers provide alarm logic and LED drivers for the following alarm functions:

- capacitor protection fuse or the circuit protection fuse
- power loss
- power switch open

The following figure shows the NTLX61AA SIM functional blocks.



Note: One feed / filter circuit is shown.

Signaling

The following table shows the signal and pinouts for the NTLX61AA SIM.

(Sheet 1 of 3)

Connection number	Pin number	Signal	Description
J1	2A, 2E, 3A-8E, 9A-9C	L-(FLT)	-48/-60 V dc (30 A max) power out
	9D, 9E	SIMHOT	-48/-60 V dc (2 A max) to mate SIM
	12D, 12E	SIMRTN	0 V dc (2 A max) to mate SIM
	12A-12C, 13A-17E, 18A, 18E	L+(FLT)	0 V dc (30 A max) power out
J2	2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 6A, 6B, 7A, 7B, 8A, 8B, 9A, 9B, 10A, 10B, 11A, 11B, 12A, 12B, 13A, 13B, 14A, 14B, 15A, 15B, 16A, 16B, 17A, 17B, 18A, 18B	LGND	0 V dc (logic ground)
	2E	REDCNTL	+3.3 V dc --> LGND to activate
	4E	GRNCNTL	+3.3 V dc --> LGND to activate
	6E	SHFL	+3.3 V dc --> LGND to activate
	8E	LEDTST	O/C --> LGND on test
	10E	FLTALM	LGND --> O/C on alarm
	12E	COOLFAIL	O/C --> on alarm
	14E	PCIUFAIL	O/C --> on alarm
	16E	SPARE1	reserved for future use
	18E	SPARE2	reserved for future use
J3	2E	JTAG1	Installation test access to shelf (not for use in service)

NTLX61AA SIM (continued)

(Sheet 2 of 3)

Connection number	Pin number	Signal	Description
	4E	JTAG2	Installation test access to shelf (not for use in service)
	6E	JTAG3	Installation test access to shelf (not for use in service)
	8E	JTAG4	Installation test access to shelf (not for use in service)
	10E	JTAG5	Installation test access to shelf (not for use in service)
	12E	JTAG6	Installation test access to shelf (not for use in service)
	14E	JTAG7	Installation test access to shelf (not for use in service)
	16E	JTAG8	Installation test access to shelf (not for use in service)
	18E	JTAG9	Installation test access to shelf (not for use in service)
J4	2A-8E	FGND	0 V DC (frame ground)
P1	A1	L-(IN)	-48/-60 V dc (30 A max) power in
	A2	L+(IN)	0 V dc (30 A max) power in
	1	DISCH	0 V dc (20 mA max)
	2	SHLFFAIL	NC
	3	LEDTEST	-48/-60 V dc --> 0 V dc on test
	4	CUFAIL	O/C (-48/-60 V dc)--> O/C (-48/-60 V dc) on alarm
	5	BIPFAIL	O/C (-48/-60 V dc)--> 0 V dc on alarm
P2	1	JTAG5	Installation test access to shelf (not for use in service)
	2	JTAG4	Installation test access to shelf (not for use in service)

(Sheet 3 of 3)

Connection number	Pin number	Signal	Description
	3	JTAG3	Installation test access to shelf (not for use in service)
	4	JTAG2	Installation test access to shelf (not for use in service)
	5	JTAG1	Installation test access to shelf (not for use in service)
	6	JTAG6	Installation test access to shelf (not for use in service)
	7	JTAG7	Installation test access to shelf (not for use in service)
	8	JTAG8	Installation test access to shelf (not for use in service)
	9	JTAG9	Installation test access to shelf (not for use in service)

NTLX63AA CEM

Description

The NTLX63AA common equipment module (CEM) provides the centralized resources required to support DMS-Spectrum Peripheral Module (SPM) applications.

ATTENTION
The NTLX63AA CEM is not compatible with SP15 or later software. Upgrade to an NTLX82AA or NTLX82BA CEM for SP15 or later software.

Location

The two NTLX63AA CEMs are located in slots 7 and 8 on shelf 0 of the NTLX51AA or NTLX51BA dual-shelf assembly.

Functions

The NTLX63AA CEM pair provides the following functions:

- bandwidth allocation
- communication and messaging
- computing platform
- network synchronization and timing subsystem
- 1 + 1 redundancy

Functional blocks

The NTLX63AA CEM has the following functional blocks:

- C-side interface
- P-side interface
- bandwidth allocator (selection)
- bandwidth allocator (distribution)
- timeswitch and pad
- messaging platform
- computing platform
- timing distribution and switch of activity (SWACT)
- power distribution

C-side interface

The C-side interface is partitioned into two areas: the channel supervision and messaging (CSM) system and the quad link chip (QLC). Within the C-side block there are nine PCM data buses.

To control possible errors, the messaging buses use cyclic redundancy check (CRC) error detection and correction, while the other buses use a proprietary parity scheme.

P-side interface

The NTLX63AA CEMs provide three serial links (S-link) for each resource module (RM). Each S-link provides 256 timeslots. Each RM can access three S-links (an S-link cluster), which provides a total of 768 timeslots.

Bandwidth allocator (selection)

The following selector functions are provided by the bandwidth allocator:

- serial link
- PCI8 local bus processor interface
- timeswitch data and control interfaces
- programmable intermodule communication
- diagnostics

Bandwidth allocator (distribution)

The bandwidth allocator (distribution) complements the selection function. It receives input from four 4,096-channel buses and outputs a 12,288-channel aggregate to six serial link interfaces. In addition, it outputs one 4,096-channel bus to the C-side transmit interface.

The 4,096-channel bus to the C-side transmit interface block is divided into 2,048 channels for payload and 2,048 channels for test pattern, pseudo-random bit sequencing (PRBS), and other functions.

The distribution functions include

- serial link output
- PCI8 local bus processor interface
- pad interface
- programmable intermodule communication
- diagnostics

NTLX63AA CEM (continued)

Timeswitch and pad

The timeswitch provides the following:

- nonblocking double buffered ports
- 12,288 input ports
- 11,264 output ports
- ROM controlled pad values
- input channel broadcast (1:n broadcast)
- NX DS-0 (hyper channel) connections
- frame integrity

Messaging platform

The messaging platform provides the following:

- 32 individually programmable full duplex physical ports
- communications using ST- and C-buses
- ST-BUS loop back for fault sectionalization
- internal fault detection and notification

Computing platform

The computing platform provides the computing resources for the SPM system.

Timing distribution and SWACT

This timing distribution and SWACT function provides the subsystem timing strobes (frame pulses), clocks, and the SWACT control subsystem.

Timing distribution

The NTLX63AA CEMs require 24.576 MHz and 32.678 MHz clock signals to operate. These clocks are generated in the timing distribution function by a dual frequency, voltage-controlled crystal oscillator (VCXO) based digital phase locked loop.

Synchronization

The common common equipment modules (CEM) form the center of a duplicated star topology. These modules are the primary synchronization distribution mechanism within the SPM system. Resource modules derive the system clock from the S-links of the active CEM.

The system clocks in the CEMs are locked to one of the following sources:

- ENET DS-512S
- mate CEM
- 8-kHz reference signal supplied to an RM in either OC3 slot

Mode of operation

The SPM synchronization architecture is capable of operating in the base or loop-timed modes.

Base mode

SPM is locked to a designated ENET plane: the other ENET plane is available as an alternate source. The phase-locked loop (PLL) oscillator in the active CEM forms the basis of the system clock. This mode is not suitable for use with SONET. However, this mode is used for timing when maintenance actions are performed on the SPM.

Loop-timed mode

Each active SPM CEM synchronizes to a clock signal received at either of the two OC3 carriers that terminate on the OC3 RM. The inactive CEM derives its clock signal from the active CEM. The SPM is locked to a frame signal received on one of the NTLX71AA OC3 interface modules that is located in one of the two OC3 slots; the signal at the other OC3 slot is available as an alternate source. The PLL oscillator in the active CEM provides the local clock. Local clock quality is determined by the CEM oscillator. This timing mode does not meet SONET requirements when both references are lost (such as holdover mode).

SWACT subsystem

Each NTLX63AA CEM generates and receives the following indications so that the standby and active CEMs are synchronized.

- mate presence
- mate failed
- mate activity indicator
- mate frame pulse (8 kHz and superframe pulses)
- mate clock status (32.768 MHz)

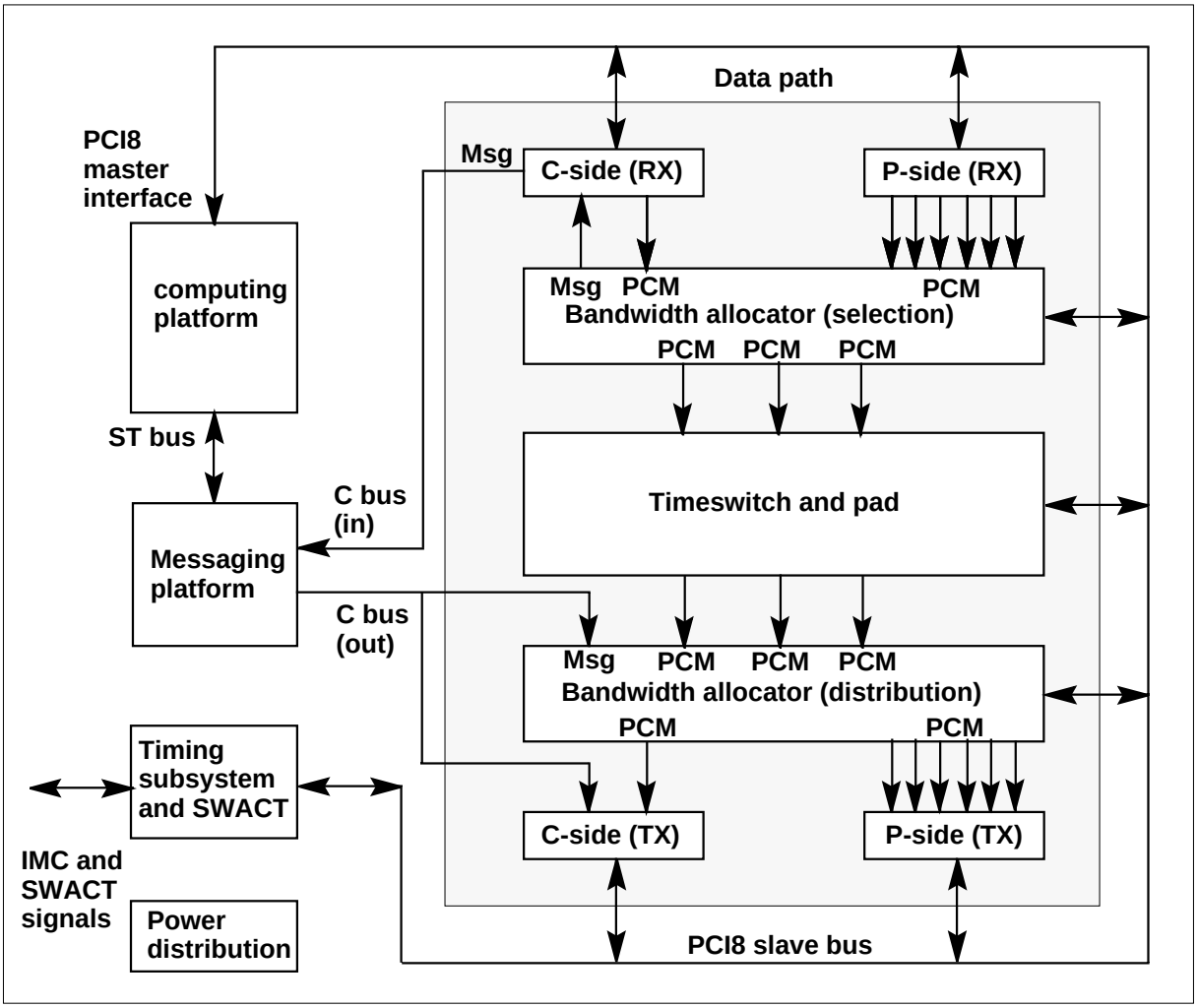
The SWACT subsystem on each NTLX63AA CEM uses the indicators to switch from one CEM to the mate CEM when required.

NTLX63AA CEM (continued)

Power distribution

The power distribution is provided by point-of-use power supplies fed from supervised dual -48 volt feeds. Primary power faults and power supply failures initiate a SWACT.

The following figure is the NTLX63AA CEM functional block diagram.



Signaling

The following table shows NTLX63AA CEM backplane connections.

(Sheet 1 of 6)

Pin	A	B	C	D	E
2	LGND	LGND	LGND	LGND	LGND
3	ToCEM_ SLOT22D2	ToCEM_ SLOT22D1	LGND	ToCEM_ SLOT23D2	ToCEM_ SLOT23D2
4	ToCEM_ SLOT22D3	ToCEM_ SLOT22CK	LGND	ToCEM_ SLOT23CK	ToCEM_ SLOT23D3
5	FrCEM_ SLOT22D2	FrCEM_ SLOT22D1	LGND	FrCEM_ SLOT23D1	FrCEM_ SLOT23D2
6	FrCEM_ SLOT22D3	FrCEM_ SLOT22CK	LGND	FrCEM_ SLOT23CK	FrCEM_ SLOT23D3
7	ToCEM_ SLOT21D2	ToCEM_ SLOT21D1	LGND	ToCEM_ SLOT24D1	ToCEM_ SLOT24D2
8	ToCEM_ SLOT21D3	ToCEM_ SLOT21CK	LGND	ToCEM_ SLOT24CK	ToCEM_ SLOT24D3
9	FrCEM_ SLOT21D2	FrCEM_ SLOT21D1	LGND	FrCEM_ SLOT24D1	FrCEM_ SLOT24D2
10	FrCEM_ SLOT21D3	FrCEM_ SLOT21CK	LGND	FrCEM_ SLOT24CK	FrCEM_ SLOT24D3
11	LGND	LGND	LGND	ToCEM_ SLOT25D1	ToCEM_ SLOT25D2
12	ToCEM_ SLOT20D2	ToCEM_ SLOT20D1	LGND	ToCEM_ SLOT25CK	ToCEM_ SLOT25D3
13	ToCEM_ SLOT20D3	ToCEM_ SLOT20CK	LGND	FrCEM_ SLOT25D1	FrCEM_ SLOT25d2
14	FrCEM_ SLOT20D2	FrCEM_ SLOT20D1	LGND	FrCEM_ SLOT25CK	FrCEM_ SLOT25D3
15	FrCEM_ SLOT20D3	FrCEM_ SLOT20CK	LGND	LGND	LGND

NTLX63AA CEM (continued)

(Sheet 2 of 6)

16	ToCEM_ SLOT19D2	ToCEM_ SLOT19D1	LGND	ToCEM_ SLOT26D1	ToCEM_ SLOT26D2
17	ToCEM_ SLOT19D3	ToCEM_ SLOT19CK	LGND	ToCEM_ SLOT26CK	ToCEM_ SLOT26D3
18	ToCEM_ SLOT19D2	FrCEM_ SLOT19D1	LGND	FrCEM_ SLOT26D1	FrCEM_ SLOT26D2
19	FrCEM_ SLOT19D3	FrCEM_ SLOT19CK	LGND	FrCEM_ SLOT26CK	FrCEM_ SLOT26D3
20	ToCEM_ Sp17D	ToCEM_ Sp17CK	LGND	ToCEM_ SLOT27D1	ToCEM_ SLOT27D2
21	FrCEM_ Sp17D	FrCEM_ Sp17CK	LGND	ToCEM_ SLOT27CK	ToCEM_ SLOT27D3
22	LGND	LGND	LGND	FrCEM_ SLOT27D1	FrCEM_ SLOT27D2
23	ToCEM_ SLOT18D2	ToCEM_ SLOT18D1	LGND	FrCEM_ SLOT27CK	FrCEM_ SLOT27D3
24	ToCEM_ SLOT18D3	ToCEM_ SLOT18D2	LGND	ToCEM_ SLOT28D1	ToCEM_ SLOT28D2
25	FrCEM_ SLOT18D2	FrCEM_ SLOT18D1	LGND	ToCEM_ SLOT28CK	ToCEM_ SLOT28D3
26	FrCEM_ SLOT18D3	FrCEM_ SLOT18CK	LGND	FrCEM_ SLOT28D1	FrCEM_ SLOT28D2
27	ToCEM_ SLOT17D2	ToCEM_ SLOT17D1	LGND	FrCEM_ SLOT28CK	FrCEM_ SLOT28D3
28	ToCEM_ SLOT17D3	ToCEM_ SLOT17CK	LGND	LGND	LGND
29	FrCEM_ SLOT17D2	FrCEM_ SLOT17D1	LGND	ToCEM_ SLOT14D1	ToCEM_ SLOT14D2
30	FrCEM_ SLOT17D3	FrCEM_ SLOT17CK	LGND	ToCEM_ SLOT14CK	ToCEM_ SLOT14D3
31	ToCEM_ SLOT16D2	ToCEM_ SLOT16D1	LGND	FrCEM_ SLOT14D1	FrCEM_ SLOT14D3

NTLX63AA CEM (continued)

(Sheet 3 of 6)

32	ToCEM_ SLOT16D3	ToCEM_ SLOT16CK	LGND	FrCEM_ SLOT14CK	FrCEM_ SLOT14D3
33	FrCEM_ SLOT16D2	FrCEM_ SLOT16D1	LGND	ToCEM_ SLOT13D1	ToCEM_ SLOT13D2
34	FrCEM_ SLOT16D3	FrCEM_ SLOT16CK	LGND	ToCEM_ SLOT13CK	ToCEM_ SLOT13D3
35	ToCEM_ Sp15D	ToCEM_ Sp15CK	LGND	FrCEM_ SLOT13D1	FrCEM_ SLOT13D2
36	FrCEM_ Sp15D	FrCEM_ Sp15CK	LGND	FrCEM_ SLOT13CK	FrCEM_ SLOT13D3
37	ToMATE_ QLC	FrMATE_ QLC	LGND	LGND	LGND
38	ToMATE_ RXPCM0	ToMATE_ RXPCM1	LGND	FrMATE_ RXPCM1	FrMATE_ RXPCM0
39					
40	ToMATE_ RXPCM2	ToMATE_ RXPCM3	LGND	FrMATE_ RXPCM3	FrMATE_ RXPCM2
41	ToMATE_ RXPCM4	ToMATE_ RXPCM5	LGND	FrMATE_ RXPCM5	FrMATE_ RXPCM4
42	ToMATE_ RXPCM6	ToMATE_ RXPCM7	ToMATE_ RXPCM8	FrMATE_ RXPCM7	FrMATE_ RXPCM6
43	ToMATE_ RXPCM_FPN	ToMATE_ RXPCM9	FrMATE_ RXPCM8	FrMATE_ RXPCM9	FrMATE_ RXPCM_FPN
44	ToMATE_ CSIDE	ToMATE_ RXPCM_CLK	LGND	FrMATE_ RXPCM_CLK	FrMATE_ CSIDE
45	ToMATE_ TXPCM0	ToMATE_ DS1	LGND	FrMATE_ DS1	FrMATE_ TXPCM0
46	ToMATE_ TXPCM2	ToMATE_ TXPCM1	LGND	FrMATE_ TXPCM1	FrMATE_ TXPCM2
47	ToMATE_ TXPCM4	ToMATE_ TXPCM3	LGND	FrMATE_ TXPCM3	FrMATE_ TXPCM4
48	ToMATE_ TXPCM7	ToMATE_ TXPCM5	ToMATE_ TXPCM6	FrMATE_ TXPCM5	FrMATE_ TXPCM7

NTLX63AA CEM (continued)

(Sheet 4 of 6)

49	ToMATE_ TXPCM9	ToMATE_ TXPCM8	FrMATE_ TXPCM6	FrMATE_ TXPCM8	FrMATE_ TXPCM9
50	ToMATE_ TXPCM_FPN	ToMATE_ TXPCM10	LGND	FrMATE_ TXPCM10	FrMATE_ TXPCM_FPN
51	ToMATE_ IMC0	ToMATE_ TXPCM_CLK	LGND	FrMATE_ TXPCM_CLK	FrMATE_ IMC0
52	ToMATE_ IMC2	ToMATE_ IMC1	LGND	FrMATE_ IMC1	FrMATE_ IMC2
53	ToMATE_ IMC4	ToMATE_ IMC3	LGND	FrMATE_ IMC3	FrMATE_ IMC4
54	ToMATE_ IMC_FPN	ToMATE_ IMC_CLK	ToMATE_ ACT	FrMATE_ IMC_CLK	FrMATE_ IMC_FPN
55	ToMATE_ SFPN	ToMATE_ PRES	FrMATE_ ACT	FrMATE_ PRES	FrMATE_ SFPN
56	ToMATE_ RSTREQ	ToMATE_ TOD	ToMATE_ ACTDROP	FrMATE_ TOD	FrMATE_ RSTREQ
57	ToMATE_ SYS_FPN	ToMATE_ SYS_CLK	FrMATE_ ACTDROP	FrMATE_ SYS_CLK	FrMATE_ SYS_FPN
58	LGND	LGND	ToMATE_ FAIL	LGND	LGND
59	ToCEM_ SLOT15D2	ToCEM_ SLOT15D1	FrMATE_ FAIL	ToCEM_ SLOT12D1	ToCEM_ SLOT12D2
60	ToCEM_ SLOT15D3	ToCEM_ SLOT15CK	LGND	ToCEM_ SLOT12CK	ToCEM_ SLOT12D3
61			LGND		
62	FrCEM_ SLOT15D2	FrCEM_ SLOT15D1	LGND	FrCEM_ SLOT12D1	FrCEM_ SLOT12D2
63	FrCEM_ SLOT15D3	FrCEM_ SLOT15CK	LGND	FrCEM_ SLOT12CK	FrCEM_ SLOT12D3
64	ToCEM_ Sp1D	ToCEM_ Sp1CK	LGND	ToCEM_ SLOT11D1	ToCEM_ SLOT11D2
65	FrCEM_ Sp1D	FrCEM_ Sp1CK	LGND	FrCEM_ SLOT11CK	FrCEM_ SLOT11D3
66	ToCEM_ SLOT1D2	ToCEM_ SLOT1D1	LGND	FrCEM_ SLOT11D1	FrCEM_ SLOT11D2

NTLX63AA CEM (continued)

(Sheet 5 of 6)

67	ToCEM_ SLOT1D3	ToCEM_ SLOT1CK	LGND	FrCEM_ SLOT11CK	FrCEM_ SLOT11D3
68	FrCEM_ SLOT1D2	FrCEM_ SLOT1D1	LGND	LGND	LGND
69	FrCEM_ SLOT1D3	FrCEM_ SLOT1CK	SYNC_FrSRMO	ToCEM_ SLOT10D7	ToCEM_ SLOT10D8
70	ToCEM_ SLOT2D2	ToCEM_ SLOT2D1	LGND	ToCEM_ SLOT10CK3	ToCEM_ SLOT10D9
71	ToCEM_ SLOT2D3	ToCEM_ SLOT2CK	LGND	FrCEM_ SLOT10D7	FrCEM_ SLOT10D8
72	FrCEM_ SLOT2D2	FrCEM_ SLOT2D1	LGND	FrCEM_ SLOT10CK3	FrCEM_ SLOT10D9
73	FrCEM_ SLOT2D3	FrCEM_ SLOT2CK	LGND	ToCEM_ SLOT10D4	FrCEM_ SLOT10D5
74	LGND	LGND	LGND	ToCEM_ SLOT10CK2	ToCEM_ SLOT10D6
75	ToCEM_ Sp3D	ToCEM_ Sp3CK	SYNC_FrOC3_ 1	FrCEM_ SLOT10D4	FrCEM_ SLOT10D5
76	FrCEM_ Sp3D	FrCEM_ Sp3CK	LGND	FrCEM_ SLOT10CK2	FrCEM_ SLOT10D6
77	ToCEM_ SLOT3D2	ToCEM_ SLOT3D1	LGND	ToCEM_ SLOT10D1	ToCEM_ SLOT10D2
78	ToCEM_ SLOT3D3	ToCEM_ SLOT3CK	SYNC_FrSRM_ 1	ToCEM_ SLOT10CK1	ToCEM_ SLOT10D3
79	FrCEM_ SLOT3D2	FrCEM_ SLOT3D1	LGND	FrCEM_ SLOT10D1	FrCEM_ SLOT10D2
80	FrCEM_ SLOT3D3	FrCEM_ SLOT3CK	LGND	FrCEM_ SLOT10CK1	FrCEM_ SLOT10D3
81	ToCEM_ SLOT4D2	ToCEM_ SLOT4D1	LGND	LGND	LGND
82	ToCEM_ SLOT4D3	ToCEM_ SLOT4CK	CEM_SLOT_ID	ToCEM_ SLOT9D7	ToCEM_ SLOT9D8

NTLX63AA CEM (continued)

(Sheet 6 of 6)

83	FrCEM_ SLOT4D2	FrCEM_ SLOT4D1	LGND	ToCEM_ SLOT9CK3	ToCEM_ SLOT9D9
84	FrCEM_ SLOT4D3	FrCEM_ SLOT4CK	BKPLN_ID3	FrCEM_ SLOT9D7	FrCEM_ SLOT9D8
85	LGND	LGND	LGND	FrCEM_ SLOT9CK3	FrCEM_ SLOT9D8
86	ToCEM_ SLOT5D2	ToCEM_ SLOT5D1	SYNC_FrOC3_ 0	ToCEM_ SLOT9D4	ToCEM_ SLOT9D5
87	ToCEM_ SLOT5D3	ToCEM_ SLOT5CK	LGND	ToCEM_ SLOT9CK2	ToCEM_ SLOT9D6
88	FrCEM_ SLOT5D2	FrCEM_ SLOT5D1	BKPLN_ID2	FrCEM_ SLOT9D4	FrCEM_ SLOT9D5
89	FrCEM_ SLOT5D3	FrCEM_ SLOT5CK	LGND	FrCEM_ SLOT9CK2	FrCEM_ SLOT9D6
90	ToCEM_ SLOT6D2	ToCEM_ SLOT6D1	BKPLN_ID1	ToCEM_ SLOT9D1	ToCEM_ SLOT9D2
91	ToCEM_ SLOT6D3	ToCEM_ SLOT6CK	LGND	ToCEM_ SLOTCK1	ToCEM_ SLOT9D3
92	FrCEM_ SLOT6D2	FrCEM_ SLOT6D1	BKPLN_ID0	FrCEM_ SLOT9D1	FrCEM_ SLOT9D2
93	FrCEM_ SLOT6D3	FrCEM_ SLOT6CK	LGND	FrCEM_ SLOT9CK1	FrCEM_ SLOT9D3
94	LGND	RED_LEDCTL_ A	LGND	RED_LEDCTL_ B	PCIU_FAIL
95	GREEN_LEDC TL_A	SHLFL_A	CUFAIL	SHLFL_B	GREEN_LEDC TL_B
96	FRAMELEDTS T	PRES_OPER_ A	MCTL	PRES_OPER_ B	LGND
97	MEN	MPR	LGND	MCLK	SPR1
98	MMD	LGND	LGND	LGND	MSD

NTLX63AA CEM (end)

The following table shows the NTLX63AA CEM power pinning.

Pin	A	B	C	D	E
2	-48B	-48B	-48B	-48B	-48B
3	NC	NC	NC	NC	NC
4	NC	NC	NC	NC	NC
5	RTN	RTN	RTN	RTN	RTN
6	NC	NC	NC	NC	NC
7	NC	NC	NC	NC	NC
8	-48A	-48A	-48A	-48A	-48A

Power requirements

The following table shows the NTLX63AA CEM general power requirements.

Parameter	Minimum	Nominal	Maximum	Units	Comments
Supply voltage	4.75	5.00	5.25	V	
Supply voltage				V	
Supply ripple				mV	
Supply current					
Power					Maximum allowed for 56 mm module

NTLX65BA DSP RM

Description

The NTLX65BA digital signal processor (DSP) resource module (RM) provides digital signal processing services for the Spectrum Peripheral Module (SPM).

Refer to “Provisioning DSP resources for the IEC market" later in this module for detailed information about provisioning DSP resources.

Location

The NTLX65BA DSP RM optionally occupies slots 9 through 13 on shelf 1 of the NTLX51BA dual-shelf assembly. The quantities and locations of the NTLX65BA DSP RM are office dependent.

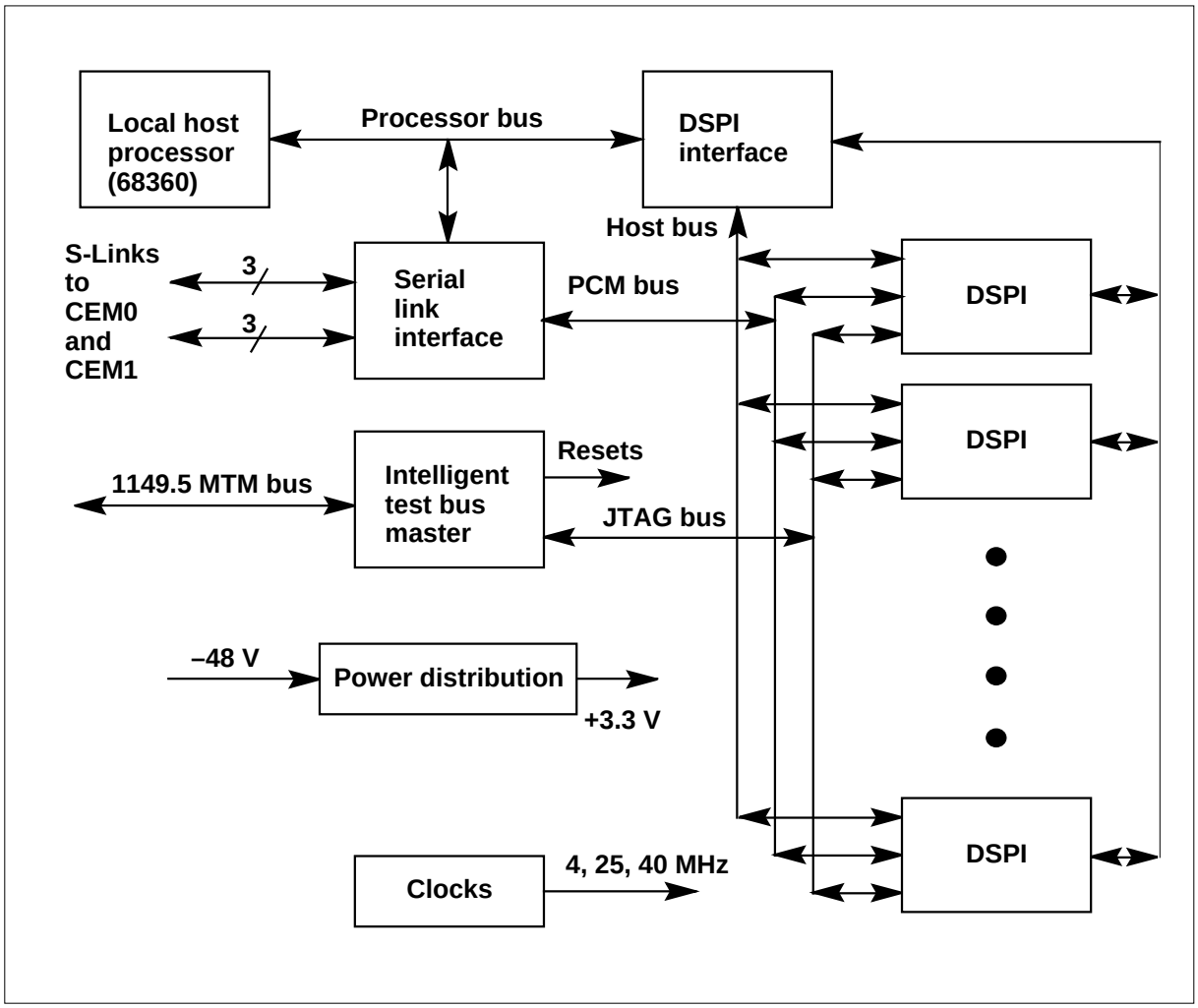
Functional blocks

The NTLX65BA DSP RM has the following functional blocks:

- computing platform
- serial link interface
- intelligent test bus master (ITM)
- clocks
- power distribution
- digital signal processor island (DSPI) interface
- DSPI

The following figure shows the functional block diagram of the NTLX65BA DSP RM.

NTLX65BA DSP RM (continued)



Computing platform

The computing platform is the NTLX65BA DSP RM central processing complex. It contains built-in serial communication controllers, dynamic random access memory, timers, debug port, and direct memory access controllers. Software loads are contained in flash-erasable programmable read-only memory (EPROM), which load directly to random access memory (RAM).

Serial link interface

The serial link interface provides messaging and pulse code modulation interfaces between the two common equipment module (CEM) and the host processor.

NTLX65BA DSP RM (continued)

ITM

The ITM consists of module information memory (MIM) and power-up reset logic.

Clock

The clock provides 4, 25, and 40 MHz clock streams. The 25 MHz clock is used by the host processor and the serial link interface. The 4 and 40 MHz clocks are used by the DSPIs.

Power distribution

The power distribution is a point of use -48 to +3 volt dc-to-dc converter and the associated filters needed to provide power to the other functions.

DSPI interface

The DSPI interface block provides the following services for the DSPI processors:

- address and data buffering
- address decoding
- DSPI interrupt consolidation
- data transfer acknowledge (DTACK) signal consolidation

DSPI

The NTLX65BA DSP RM contains nine DSP islands that consist of the following:

- DSPI application-specific integrated circuit (ASIC)
- DSP microprocessor
- 128 kilobytes of static random access memory

The DSPIs provide tone generation through the use of digital signal processing.

Signaling

The following table provides the NTLX65BA DSP RM backplane pin descriptions.

(Sheet 1 of 2)

Signal	Function	IO Type	Description
-48A	power	-	-48 V battery feed A
-48B	power	-	-48 V battery feed B

(Sheet 2 of 2)

Signal	Function	IO Type	Description
RTN	power	-	Battery return
FrCEMnCK	input	3.3V CMOS SLIF-S	S-link clock lines from common equipment (n = 0 CEM0, n = 1 CEM1)
FrCEMnDm	input	3.3V CMOS SLIF-S	S-link clock lines from common equipment (n = 0 CEM0, n = 1 CEM1, m = 1, 2, 3)
ToCEMnCK	output	3.3V CMOS SLIF-S	S-link clock lines from common equipment (n = 0 CEM0, n = 1 CEM1)
ToCEMnDM	output	3.3V CMOS SLIF-S	S-link clock lines from common equipment (n = 0 CEM0, n = 1 CEM1, m = 1, 2, 3)
MMD	input	3.3V CMOS ITM	JTAG 1149.5 bus master data
MSD	input/output open drain	3.3V CMOS ITM	JTAG 1149.5 bus slave data
MCLK	input	3.3V CMOS ITM	JTAG 1149.5 bus clock
MPR	input output open drain	3.3V CMOS ITM	JTAG 1149.5 bus request
MCT	input	3.3V CMOS ITM	JTAG 1149.5 bus control
SLOT_IDn	input	GND/NC	RM slot ID (n = 0, 1, 2, 3, 4) (pin is either grounded on the backplane or floating)
LGND	power	-	Logic ground of the PCP/BACKPLANE

The following table provides the NTLX65BA DSP RM backplane 1SU power connector pin descriptions.

(Sheet 1 of 2)

Pin	A	B	C	D	E
2	-48B	-48B	-48B	-48B	-48B
3	NC	NC	NC	NC	NC
4	NC	NC	NC	NC	NC
5	RTN	RTN	RTN	RTN	RTN
6	NC	NC	NC	NC	NC

NTLX65BA DSP RM (continued)

(Sheet 2 of 2)

Pin	A	B	C	D	E
7	NC	NC	NC	NC	NC
8	-48A	-48A	-48A	-48A	-48A

The following table provides the NTLX65BA DSP RM backplane 2SU power connector pin descriptions.

(Sheet 1 of 2)

Pin	A	B	C	D	E
2	SYNC_toCEM0	LGND	LGND	LGND	SYNC_FrOC30
3	SYNC_toCEM1	ToSRM_Mate	LGND	FrSRM_Mate	SYNC_FrOC31
4	LGND	LGND	LGND	LGND	LGND
5	ToCEM0_SpD	ToCEM0_SpCK	LGND	ToCEM1_SpCK	ToCEM1_SpD
6	FrCEM0_SpD	FrCEM0_SpCK	LGND	FrCEM1_SpCK	FrCEM1_SpD
7	ToCEM0_D2	ToCEM0_D1	LGND	ToCEM1_D1	ToCEM1_D2
8	ToCEM0_D3	ToCEM0_CK	LGND	ToCEM1_CK	ToCEM1_D3
9	FrCEM0_D2	FrCEM0_D1	LGND	FrCEM1_D1	FrCEM1_D2
10	FrCEM0_D3	FrCEM0_CK	LGND	FrCEM1_CK	FrCEM1_D3
11	LGND	LGND	LGND	LGND	LGND
12	See Note 4.	See Note 4.	LGND	See Note 4.	See Note 4.
13	See Note 4.	See Note 4.	LGND	See Note 4.	See Note 4.
14	See Note 4.	See Note 4.	LGND	See Note 4.	See Note 4.
15	See Note 4.	See Note 4.	LGND	See Note 4.	See Note 4.
16	SLOT_ID4	SLOT_ID3	MTCL	SLOT_ID1	SLOT_ID0
17	LGND	MPR	SLOT_ID2	MCLK	LGND

(Sheet 2 of 2)

Pin	A	B	C	D	E
18	MMD	LGND	LGND	LGND	MSD

Note 1: Pins 2B, 2C, 2D, 18B, 18C, and 18D are advanced pins.

Note 2: Connections for signals at pins 2A, 2E, 3A, 3B, 3D and 3D are only made in slots 5 through 10. These are special signals distributed between the CEMs and the OC3 interface modules. These pins are left as no-connects in all other slots. These signals are not used by the DSPR.

Note 3: Spare S-links are terminated on pins 5ABDE, 6ABDE only in slots 1, 3, 15 and 17. These pins are left as no-connects in all other slots. These signals are not used by the DSP RM.

Note 4: Pins 12-15 ABDE are reserved for future use. These pins may be used to fold over the S-link connections from the adjacent DSP RM to provide increased bandwidth at a single DSP RM slot. These signals are not used by the DSP RM.

The following table provides the BDM 10-pin (2 x 5) header pin descriptions.

Pin	Signal	Signal	Pin number
1	DS	BERR	2
3	GND	BKPT/DSCLK	4
5	GND	FREEZE	6
7	RESETH	IFETCH/DSI	8
9	VDD	IPIP0/DSO	10

The following table provides the RS-232 connector pin descriptions.

Pin	Signal	Signal	Pin number
1	not used	RX	2
3	TX	not used	4
5	GND	not used	6
7	RTS/TX2	IFETCH/CTS/RX2	8
9	not used		

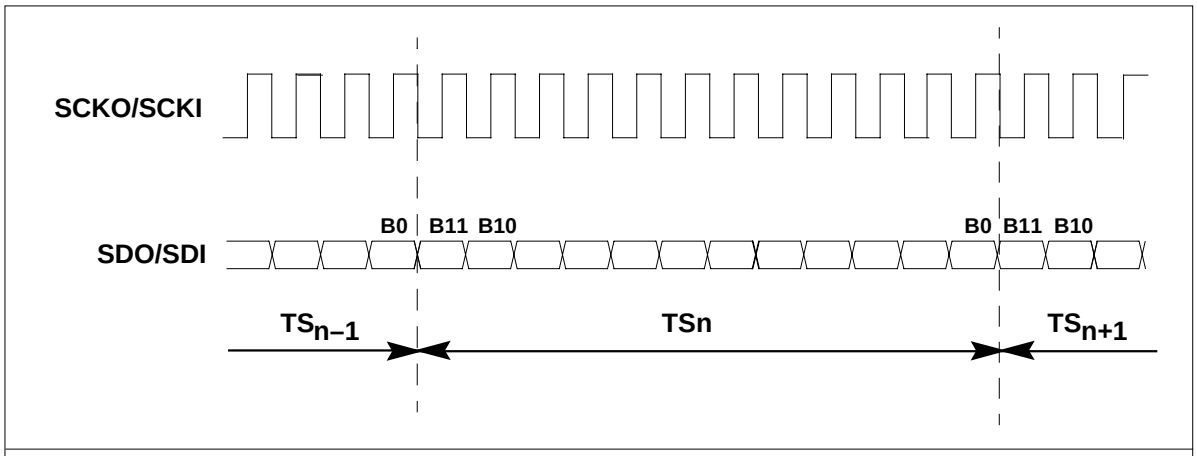
NTLX65BA DSP RM (continued)

Timing

Timing is described in the following paragraphs.

Serial link interface timing

The following figure shows serial link interface timing.

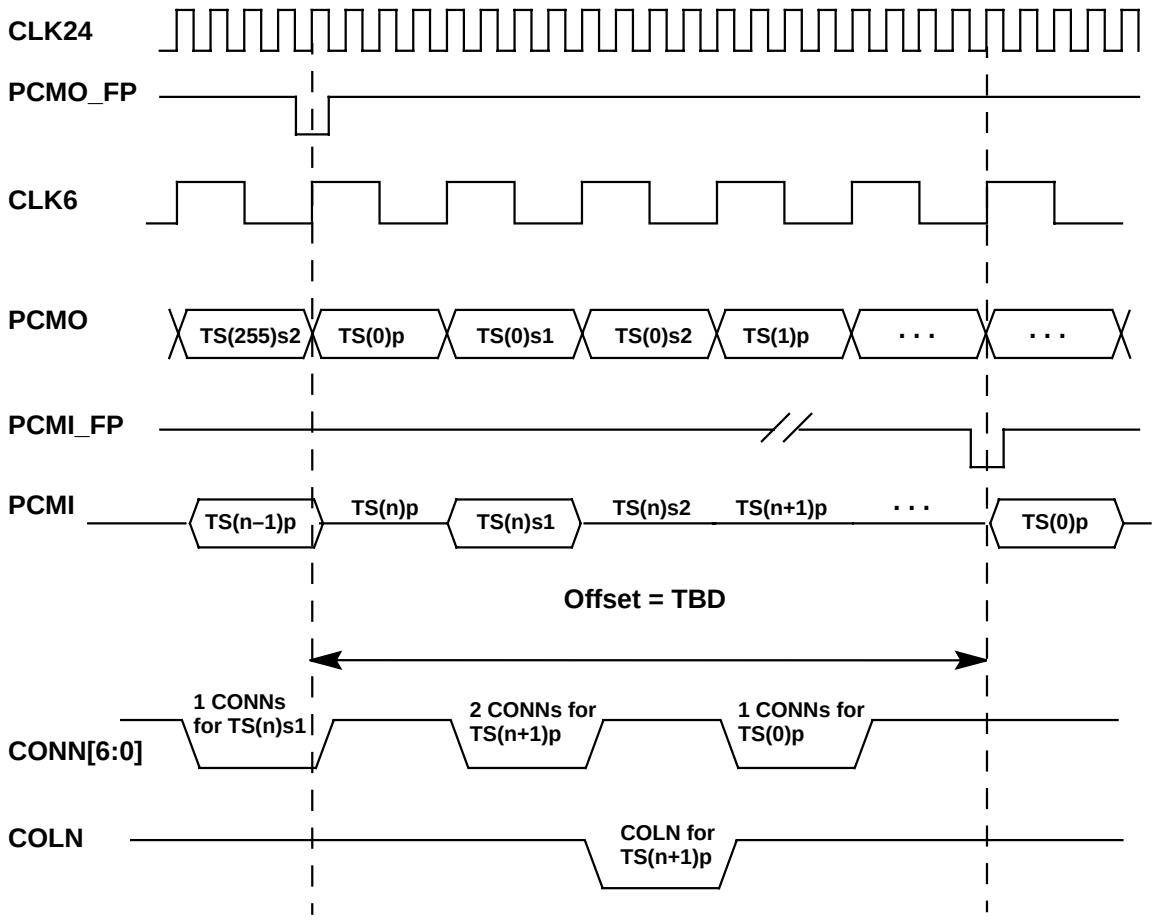


Legend:

SCKO	Serial clock out
SCKI	Serial clock in
SDO	Serial data in
SDI	Serial data out
B0, B1, B#	Bit of the serial data (each timeslot has 12 bits of data; that is Bit 0 through Bit 11)
TS	Timeslot

PCM bus timing

The following figure shows PCM bus timing.



Legend:

CLK24	24.756 MHz clock
PCMO_FP	PCM out frame pulse
CLK6	6.144 MHz clock
PCMO	PCM out (transmit)
PCMI_FP	PCM in frame pulse
PCMI	PCM in (receive)
Offset	Offset between transmit and recieve PCM frames
CONN[6:0]	Connection signals 0 through 6
COLN	Collision signal

NTLX65BA DSP RM (continued)

Power requirements

The maximum power dissipation of the NTLX65BA DSP RM does not exceed 40 watts. The following table shows the general power requirements.

Parameter	Minimum	Nominal	Maximum	Units
Supply voltage	3.10	3.30	03.50	V
Supply noise			20.00	mV
Supply current		5.0	6.0	A

Provisioning DSP resources for the IEC market

The following paragraphs describe the SPM-DSP provisioning rule for the interexchange carrier (IEC) market.

The number of DSP RMs depends on the call rate, average call holding time (or port utilization) and signaling mix. The worst case scenario for particular DSP resources is either 100% ISUP or 100% PTS. Two generic DSP RM configurations are recommended : 4+1 and 5+1.

In the 4+1 configuration, 4 DSP RMs are active and 1 DSP RM is on warm-standby ready to replace any failing active module. In the 5+1 configuration, 5 DSP RMs are active and 1 DSP RM in on warm standby. The RM sparing configuration always assumes one warm-standby RM. More specific configurations can be used to address specific requirements.

Note: Underlying assumptions in the RM provisioning calculations are:

- Call rate equal to 13.44 half-calls per second (h-CPS)
- 100% call originations, since originations require more DSP resources than terminations
- 100% MF on PTS, which is worst case assumption for the MF resources

4+1 DSP Configuration

The 4+1 configuration, shown in the table below, supports the following:

- Up to 100% COT testing
- Up to 80% call reoriginations (worst-case scenario for DTMF resources)

Resource	DSP 0	DSP 1	DSP 2	DSP 3	DSP 4	Total	DSPI's
COT	0	0	80	80	spare	160	2
Tonesyn	255	255	0	0	spare	510	2
DTMF	320	384	320	320	spare	1344	21
ABBIT	14	14	28	28	spare	84	6
MF	40	40	40	40	spare	160	4
DSPI's	8	9	9	9	Total DSPI's =		35

For the DTMF resources, which provide equivalence to XPM UTR/GTR functionality, there are

- 320 resources occupying 5 islands on DSP 0
- 384 resources occupying 6 islands on DSP 1
- 320 resources occupying 5 islands on DSP 2
- 320 resources occupying 5 islands on DSP 3
- for a grand total of 1344 DTMF resources, which could support up to 1344 originations.

Note: The DTMF resources are also used for mid-call features, such as reorigination, that are shared with mid-call events.

NTLX65BA DSP RM (end)

5+1 DSP Configuration

The 5+1 configuration, shown in the table below, supports the following:

- Up to 100% COT testing
- Up to 100% call reoriginations

Resource	DSP 0	DSP 1	DSP 2	DSP 3	DSP 4	DSP 5	Total	DSPI's
COT	0	80	0	80	0	spare	160	2
Tonesyn	255	0	255	0	0	spare	510	2
DTMF	320	320	320	320	384	spare	1664	26
ABBIT	14	14	14	14	28	spare	84	6
MF	40	40	40	40	0	spare	160	4
DSPI's	8	8	8	8	8	Total DSPI's =		40

For the DTMF resources there are

- 320 resources occupying 5 islands on DSP 0
- 320 resources occupying 5 islands on DSP 1
- 320 resources occupying 5 islands on DSP 2
- 320 resources occupying 5 islands on DSP 3
- 384 resources occupying 5 islands on DSP 4
- for a grand total of 1664 DTMF resources, which could support up to 1664 originations.

Note: The DTMF resources are also used for mid-call features, such as reorigination, that are shared with mid-call event.

NTLX66BA VSP RM

Description

The NTLX66BA voice signal processor (VSP) resource module (RM) provides resources for call processing such as echo cancellation for the DMS-Spectrum Peripheral Module (SPM). The VSP RM architecture is similar to the NTLX65BA digital signal processor (DSP) RM.

ATTENTION
The voice signal processor (VSP) does not apply to all markets.

Location

The NTLX66BA VSP RM optionally occupies slots 3 through 4 and 11 through 14 on shelf 0, and slots 5 through 6 and 14 on shelf 1 of the NTLX51BA dual-shelf assembly. The quantities and locations of VSP RMs are office dependent.

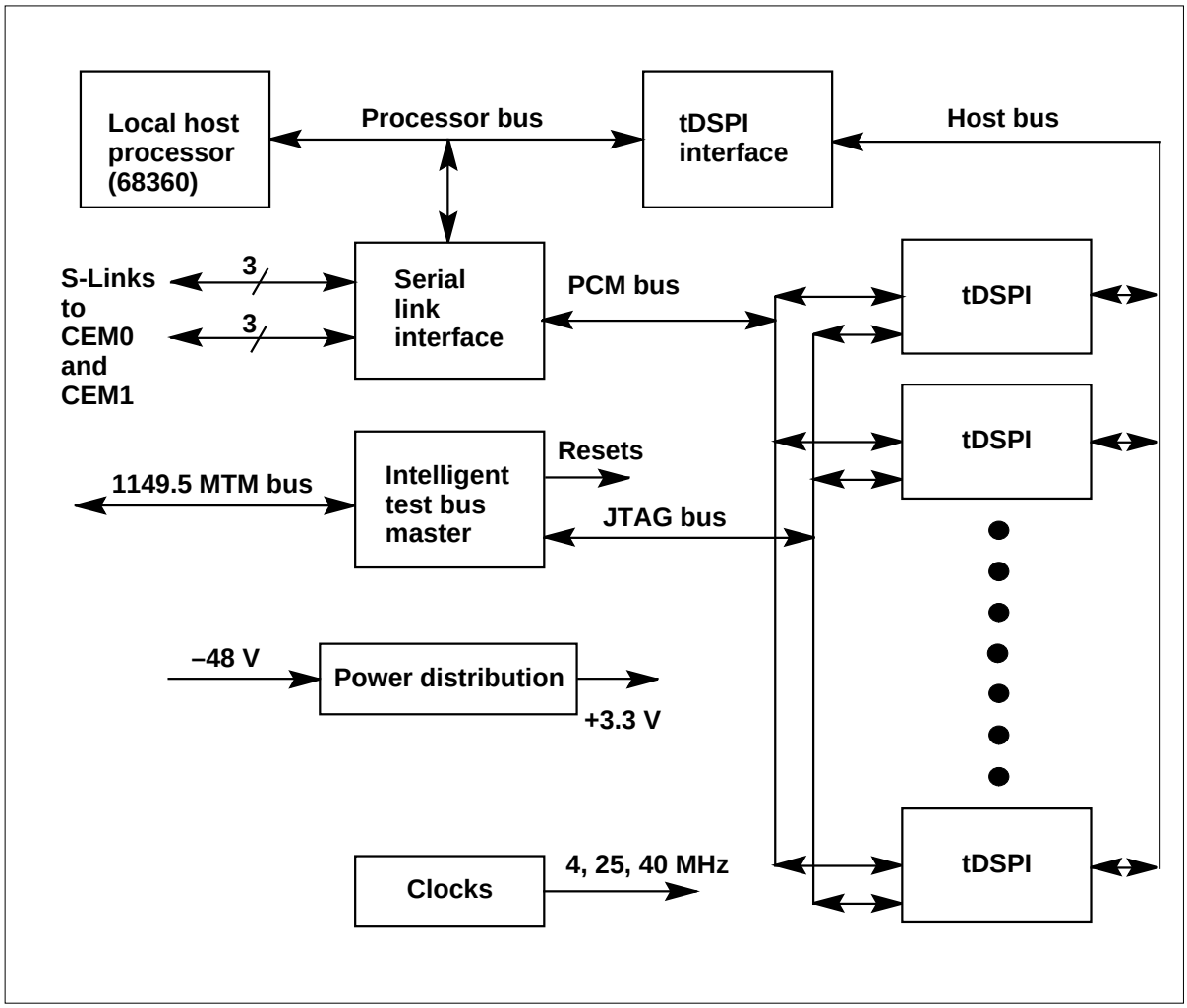
Functional blocks

The NTLX66BA VSP RM has the following functional blocks:

- computing platform
- serial link interface
- intelligent test bus master (ITM)
- clocks
- power distribution
- DSPI interface
- tDSPI

The following figure shows the functional block diagram of the VSP RM.

NTLX66BA VSP RM (continued)



Computing platform

The computing platform is the NTLX66BA VSP RM central processing complex. It contains built-in serial communication controllers, dynamic random access memory, timers, debug port, and direct memory access controllers. Software loads are contained in flash-erasable programmable read-only memory (EPROM), which load directly to random access memory (RAM).

Serial link interface

The serial link interface provides messaging and pulse code modulation interfaces between the two common equipment modules (CEM) and the host processor.

ITM

The ITM consists of module information memory (MIM), and power-up reset logic.

Clock

The clock provides 4, 25, and 40 MHz clock streams. The 25 MHz clock is used by the host processor and the serial link interface. The 4 and 40 MHz clocks are used by the digital signal processor islands (DSPI).

Power distribution

The power distribution function uses a -48 to +3 volt dc-to-dc converter and its associated filters to provide power to the other functions.

DSPI interface

The DSPI interface block provides the following services for the host processor the turbo (t) DSPI (tDSPI):

- address and data buffering
- address decoding
- DSPI interrupt consolidation
- data transfer acknowledge (DTACK) signal consolidation

tDSPI

The VSP RM contains ten tDSP islands that consist of the following functions and devices:

- tDSPI ASIC
- tDSP microprocessor
- 128 kilobytes of static random access memory

Signaling

The following table lists the NTLX66BA VSP RM backplane pin description.

(Sheet 1 of 2)

Signal	Function	IO Type	Description
-48A	power	-	-48 V battery feed A
-48B	power	-	-48 V battery feed B
RTN	power	-	Battery return

NTLX66BA VSP RM (continued)

(Sheet 2 of 2)

Signal	Function	IO Type	Description
FrCEMnCK	input	3.3V CMOS SLIF-S	S-link clock lines from common equipment (n = 0 CEM0, n = 1 CEM1)
FrCEMnDm	input	3.3V CMOS SLIF-S	S-link clock lines from common equipment (n = 0 CEM0, n = 1 CEM1, m = 1, 2, 3)
ToCEMnCK	output	3.3V CMOS SLIF-S	S-link clock lines from common equipment (n = 0 CEM0, n = 1 CEM1)
ToCEMnDM	output	3.3V CMOS SLIF-S	S-link clock lines from common equipment (n = 0 CEM0, n = 1 CEM1, m = 1, 2, 3)
MMD	input	3.3V CMOS ITM	JTAG 1149.5 bus master data
MSD	input/output open drain	3.3V CMOS ITM	JTAG 1149.5 bus slave data
MCLK	input	3.3V CMOS ITM	JTAG 1149.5 bus clock
MPR	input output open drain	3.3V CMOS ITM	JTAG 1149.5 bus request
MCT	input	3.3V CMOS ITM	JTAG 1149.5 bus control
SLOT_IDn	input	GND/NC	RM slot ID (n = 0, 1, 2, 3, 4) (pin is either grounded on backplane or floating)
LGND	power	-	Logic ground of the PCP/BACKPLANE

The following table lists the NTLX66BA VSP RM backplane 1SU power connector pin description.

(Sheet 1 of 2)

Pin	A	B	C	D	E
2	-48B	-48B	-48B	-48B	-48B
3	NC	NC	NC	NC	NC
4	NC	NC	NC	NC	NC
5	RTN	RTN	RTN	RTN	RTN
6	NC	NC	NC	NC	NC

(Sheet 2 of 2)

Pin	A	B	C	D	E
7	NC	NC	NC	NC	NC
8	-48A	-48A	-48A	-48A	-48A

The following table lists the NTLX66BA VSP RM backplane 2SU power connector pin description.

(Sheet 1 of 2)

Pin	A	B	C	D	E
2	SYNC_toCEM0	LGND	LGND	LGND	SYNC_FrOC30
3	SYNC_toCEM1	ToSRM_Mate	LGND	FrSRM_Mate	SYNC_FrOC31
4	LGND	LGND	LGND	LGND	LGND
5	ToCEM0_SpD	ToCEM0_SpCK	LGND	ToCEM1_SpCK	ToCEM1_SpD
6	FrCEM0_SpD	FrCEM0_SpCK	LGND	FrCEM1_SpCK	FrCEM1_SpD
7	ToCEM0_D2	ToCEM0_D1	LGND	ToCEM1_D1	ToCEM1_D2
8	ToCEM0_D3	ToCEM0_CK	LGND	ToCEM1_CK	ToCEM1_D3
9	FrCEM0_D2	FrCEM0_D1	LGND	FrCEM1_D1	FrCEM1_D2
10	FrCEM0_D3	FrCEM0_CK	LGND	FrCEM1_CK	FrCEM1_D3
11	LGND	LGND	LGND	LGND	LGND
12	See Note 4.	See Note 4.	LGND	See Note 4.	See Note 4.
13	See Note 4.	See Note 4.	LGND	See Note 4.	See Note 4.
14	See Note 4.	See Note 4.	LGND	See Note 4.	See Note 4.
15	See Note 4.	See Note 4.	LGND	See Note 4.	See Note 4.
16	SLOT_ID4	SLOT_ID3	MTCL	SLOT_ID1	SLOT_ID0
17	LGND	MPR	SLOT_ID2	MCLK	LGND

NTLX66BA VSP RM (continued)

(Sheet 2 of 2)

Pin	A	B	C	D	E
18	MMD	LGND	LGND	LGND	MSD

Note 1: Pins 2B, 2C, 2D, 18B, 18C, and 18D are advanced pins.

Note 2: Connections for signals at pins 2A, 2E, 3A, 3B, 3D and 3D are only made in slots 5 through 10. These are special signals distributed between the CEMs and the OC3 RMs. These pins are left as no-connects in all other slots. These signals are not used by the VSP RM.

Note 3: Spare S-links are terminated on pins 5ABDE, 6ABDE only in slots 1, 3, 15 and 17. These pins are left as no-connects in all other slots. These signals are not used by the VSP RM.

Note 4: Pins 12-15 ABDE are reserved for future use. These pins may be used to fold over the S-link connections from the adjacent RM to provide increased bandwidth at a single RM slot. These signals are not used by the VSP RM.

The following table lists the BDM 10-pin (2 x 5) header pin description.

Pin	Signal	Signal	Pin number
1	DS	BERR	2
3	GND	BKPT/DSCLK	4
5	GND	FREEZE	6
7	RESETH	IFETCH/DSI	8
9	VDD	IPIP0/DSO	10

The following table lists the RS-232 connector pin description.

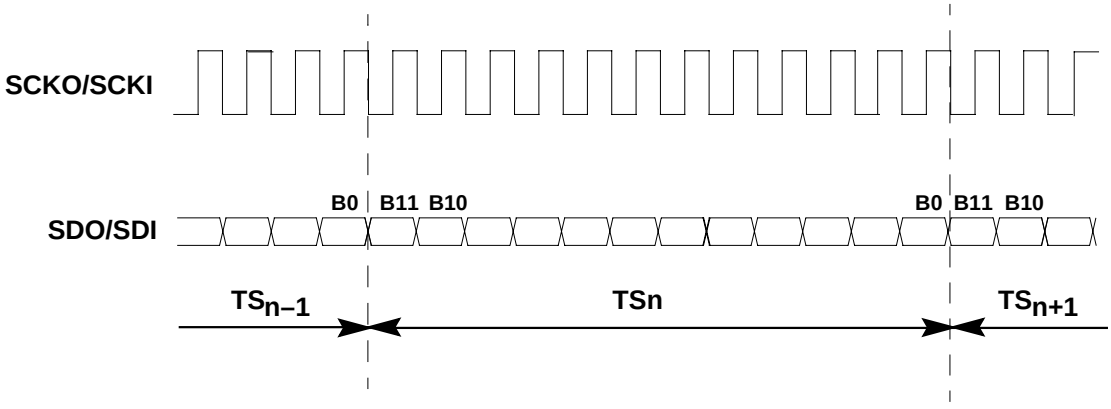
Pin	Signal	Signal	Pin number
1	not used	RX	2
3	TX	not used	4
5	GND	not used	6
7	RTS/TX2	IFETCH/CTS/RX 2	8
9	not used		

Timing

Timing is described in the following paragraphs.

Serial link interface timing

The following figure shows serial link interface timing.



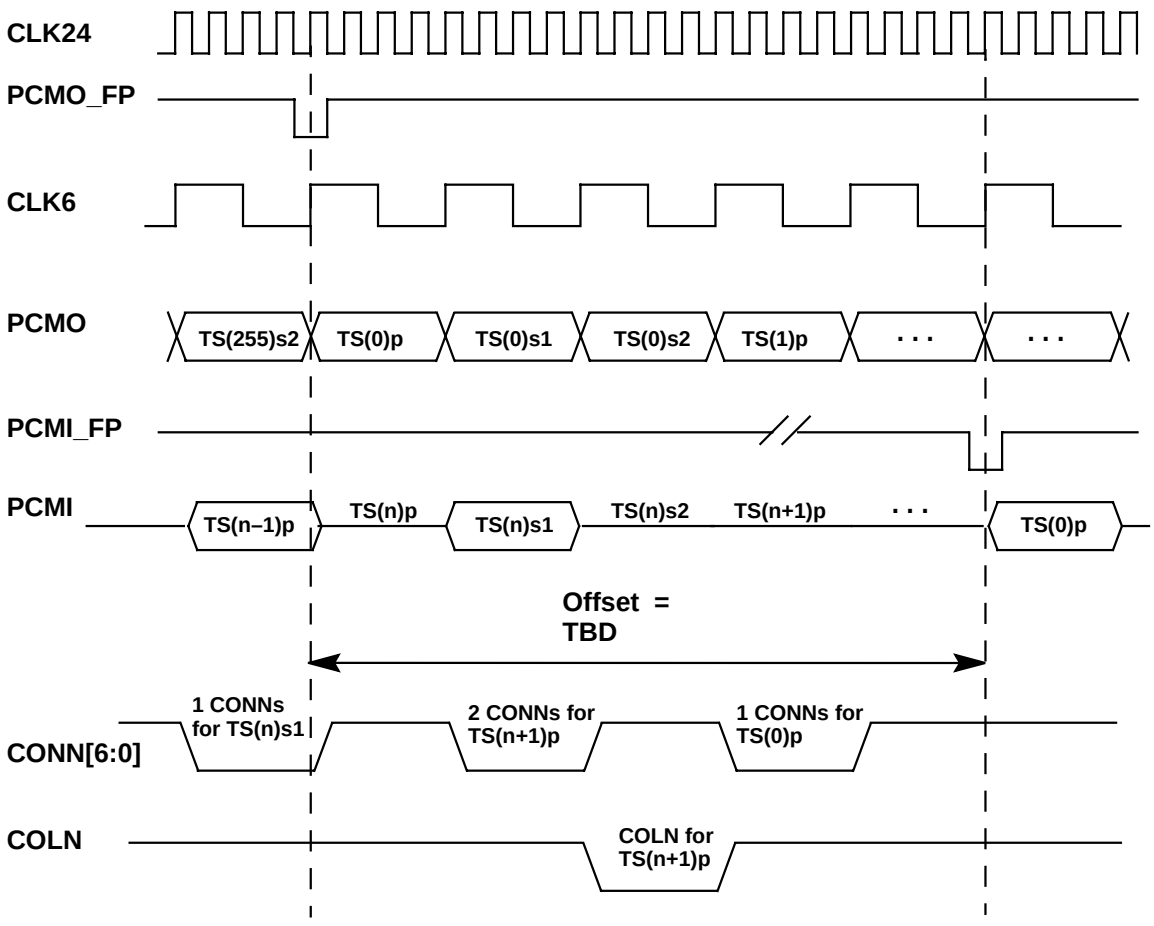
Legend:

SCKO	Serial clock out
SCKI	Serial clock in
SDO	Serial data in
SDI	Serial data out
B0, B1, B#	Bit of the serial data (each timeslot has 12 bits of data; that is Bit 0 through Bit 11)
TS	Timeslot

PCM bus timing

The following figure shows PCM bus timing.

NTLX66BA VSP RM (continued)



Legend:

CLK24	24.756 MHz clock
PCMO_FP	PCM out frame pulse
CLK6	6.144 MHz clock
PCMO	PCM out (transmit)
PCMI_FP	PCM in frame pulse
PCMI	PCM in (receive)
Offset	offset between transmit and recieve PCM frames
CONN[6:0]	connection signals 0 through 6)
COLN	collision signal

NTLX66BA VSP RM (end)

Power requirements

The maximum power dissipation of the NTLX66BA VSP RM does not exceed 40 watts. The following table shows general power requirements.

Parameter	Minimum	Nominal	Maximum	Units	Condition
Supply voltage	3.10	3.30	03.50	V	
Supply noise			20.00	mV	
Supply current		5.0	6.0	A	

NTLX71BA OC3 interface module

Description

The NTLX71BA OC3 interface module is a synchronous optical network (SONET) OC3 trunk interface module for the DMS-Spectrum Peripheral Module (SPM). It allows the SPM to terminate SONET OC3 transmission systems carrying DS3, asynchronous VT1.5, and byte-synchronous VT1.5 payloads.

Location

The NTLX71BA OC3 interface module occupies slots 9 and 10 on shelf 0 in NTLX51BA dual-shelf assembly.

Functions

The NTLX71BA OC3 interface module provides the following services:

- SONET OC3 interface with DS3, floating asynchronous VT1.5, and floating byte synchronous VT1.5.
- SONET alarm support
- DS0 trunk conditioning support

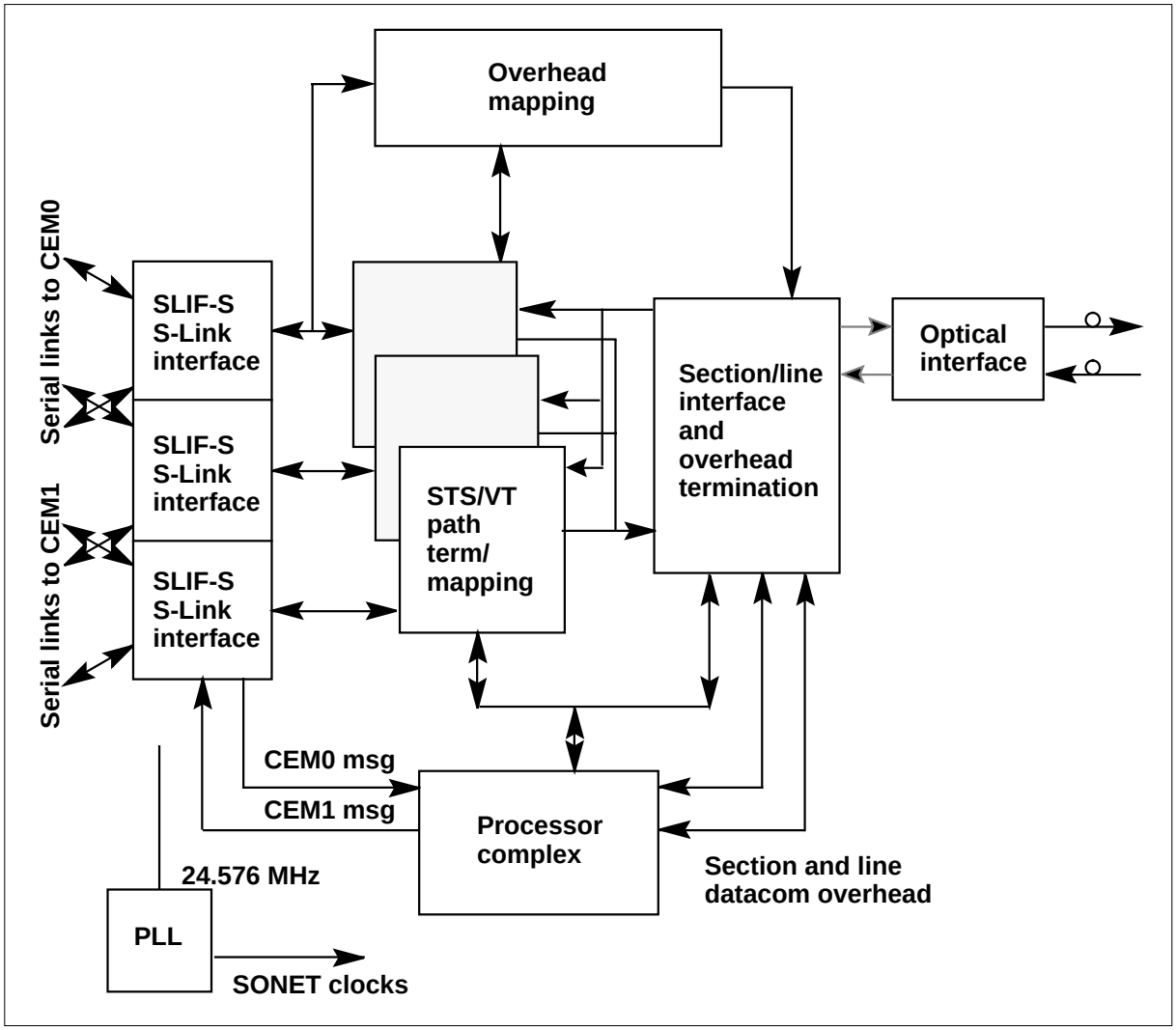
Functional blocks

The NTLX71BA OC3 interface module has the following functional blocks:

- optical interface
- section/line interface
- STS/VT path termination and mapping
- processor platform
- overhead mapping
- S-link interface
- phase lock loop

The following figure shows the NTLX71BA OC3 interface module functional block diagram.

NTLX71BA OC3 interface module (continued)



Optical interface

The NTLX71BA OC3 interface module provides an intermediate- and a long-reach OC3 optical transceiver (155.52 Mbyte/s) to terminate the physical fiber. The NTLX71BA converts the signal to an electrical format and forwards the signal to the section/line interface.

The laser output of the transmit electro-optical module can be disabled for safety during diagnostics. In addition, it is monitored for laser bias and optical output power output. The receive module provides low light and received power indications.

NTLX71BA OC3 interface module (continued)

The following tables list the optical interface specifications for the OC3 interface module.

(Sheet 1 of 2)

OC3 optical interface circuit pack specifications		
Parameter (see Note 1 and Note 2)	**1310 nm Intermediate reach**	**1310 nm Long reach**
Product engineering code	NT7E01DA/DB/DC/DD	NT7E01CA/CB/CC/CD
Connector type(see Note 3)	Biconic, FC-PC, ST/PC, SC	Biconic, FC-PC, ST/PC, SC
Pigtaill	Single mode	
General fiber type	Single mode	Single mode
Class of fiber	9.5 mm	Single mode
Mode-field diameter		9.5 mm
Optical source		
Device type	MLM	MLM
Material composition	GaAs	GaAs
Spectral characteristics		
Central wavelength	1310 nm	1310 nm
Spectral width	5 nm (D1MSTM)	5 nm (D1MSTM)
Spectral width	7.7 nm (D1RMS)	7.7 nm (D1RMS)
Central wavelength range	1260-1360 nm	1280-1335 nm
Optical signal		
LIne rate	OC3 (155.52 Mb/s)	OC3 (155.52 Mb/s)
Line code	NRZ	NRZ
Extinction ratio	8.2 dB	10 dB

NTLX71BA OC3 interface module (continued)

(Sheet 2 of 2)

OC3 optical interface circuit pack specifications		
Parameter (see Note 1 and Note 2)	**1310 nm Intermediate reach**	**1310 nm Long reach**
Optical Power		
Guaranteed launch power	-15 dBm	-5.0 dBm
Maximum launch power	-8 dBm	0 dBm

Note 1: All parameters apply on the line side of the optical connector, as specified in Bellcore Specifications TR-NWT-000253, Issue 2.

Note 2: All parameters are valid over the full range of operating, environmental, and aging conditions.

Note 3: All parameters are valid for each of the appropriate connector options.

(Sheet 1 of 2)

OC3 optical interface receiver specifications		
Parameter (See Note 1)	**1310 nm Intermediate reach**	**1310 nm Long reach**
Product engineering code	NT7E01DA/DB/DC/DD	NT7301CA/CB/CD
Connector type	Biconic, FC-PC, ST/PC, SC	Biconic, FC-PC, ST/PC, SC
Pigtail		
General fiber type	Multimode	Multimode
Optical detector		
Device type	PIN	APD
Material composition	InGaAs	III-V

Note 1: These specifications are worst-case parameters that include allowances for connector losses, aging, equipment impairments because of implementation, and temperature degradation. The values represent the power level measure at the station fiber on the link side of the connector.

Note 2: Miniature variable optical attenuators (mVOAs) may be requried at the receiver depending on the link loss. Overload level is the maximum received optical power for which BER of 10-*10* and all jitter tolerance specifications are met.

Note 3: The damage level is the maximum optical power for which no long term damage to the components will occur.

Note 4: The optical path penalty includes degradations in performance due to dispersions, reflections and optical jitter consistent with the requirements of Bellcore Specification TA-NWT-000253, Issue 2.

NTLX71BA OC3 interface module (continued)

(Sheet 2 of 2)

OC3 optical interface receiver specifications		
Parameter (See Note 1)	**1310 nm Intermediate reach**	**1310 nm Long reach**
Spectral characteristics		
Central wavelength	1265-1355 nm	1280-1335 nm
Optical signal		
Line rate	OC3 (155.52 Mb/s)	OC3 (155.52 Mb/s)
Line code	NRZ	NRZ
Overload level (See Note 2)	-8.0 dBm	-10.0 dBm
Damage level (See Note 3)	N/A	-6.0 dBm
Maximum receiver reflectance	-14.0 dB	-14.0 dB
Optical path penalty (See Note 4)	1.0 dB	1.0 dB
Optical power		
Guaranteed receiver sensitivity	-28.0 dBm	-34.0 dBm

Note 1: These specifications are worst-case parameters that include allowances for connector losses, aging, equipment impairments because of implementation, and temperature degradation. The values represent the power level measure at the station fiber on the link side of the connector.

Note 2: Miniature variable optical attenuators (mVOAs) may be requried at the receiver depending on the link loss. Overload level is the maximum received optical power for which BER of 10-*10* and all jitter tolerance specifications are met.

Note 3: The damage level is the maximum optical power for which no long term damage to the components will occur.

Note 4: The optical path penalty includes degradations in performance due to dispersions, reflections and optical jitter consistent with the requirements of Bellcore Specification TA-NWT-000253, Issue 2.

NTLX71BA OC3 interface module (continued)

OC3 optical interface guaranteed system gain specifications		
Parameter (See Note)	**1310 nm Intermediate reach**	**1310 nm Long reach**
Product engineering code	NT7E01DA/DB/DC/DD	NT7E01CA/CB/CC/CD
Attenuation	0 to 12 dB	10 to 28 dB
Optical return loss	14 dB	24 dB
Dispersion	96 ps/nm	185 ps/nm
Guaranteed launch power	-15 dBm	-5.0 dBm
Maximum transmit power	-8.0 dBm	0.0 dBm
Receiver sensitivity	-28.0 dBm	-34.0 dBm
Maximum receiver power	-8.0 dBm	-10.0 dBm
Receiver damage level	N/A	N/A
Guaranteed system gain	13.0 dB	29.0 dB

Note: These specifications are worst-case parameters that include connector losses, aging, equipment impairments because of implementation, and temperature degradation. These specifications do not include the customer unallocated link margin or the optical path penalty.

Section/line interface

The section/line interface accepts the electrical signals from the NTLX71BA OC3 interface module and handles the overhead termination through the PMC-Sierra PM5344. The PM5344 handles line defect detection, performance related overhead, protection switching overhead, and alarms.

SONET overhead not handled by the PM5343 is routed to the overhead mapping functions for additional processing.

Synchronous transport signal (STS)/virtual tributary (VT) path termination and mapping

STS termination and mapping

The STS path is terminated by the PCM-Sierra PM5344, which handles the STS pointer processing and overhead termination.

Received data is provided on the drop side of the telecom bus, along with synchronous payload envelope (SPE) and alignment indication (C1J1).

NTLX71BA OC3 interface module (continued)

In the transmit direction, the PM5344 accepts the Add side of the telecom bus from the VT and DS3 mappers.

DS1/VT termination

The three SPEs and constituent DS3 and VT1.5 structures are handled in the VT path termination and mapping section. Each of these mapping sections takes an SPE and maps the payload as DS3 or floating VT1.5. In the case of DS3, the L3M mapping device interfaces to the telecom bus and maps DS3 payloads according to SONET specifications. The DS3 signal is routed to and from an M13 multiplexing device as B3ZS signals, allowing path integrity checking. The M13 device maps 28 DS1s into a DS3 stream. The 28 DS1s are split into three groups of eight and a group of four and terminated on the octal mapping resource (OMaR) application specific integrated circuit (ASIC). Each DS1 interfaces to the M13 as a separate signal group consisting of transmit data and clock with received data and clock.

For floating VT1.5 mapped DS1 signals in the SPE, the OMaR devices interface to the demultiplexed telecom bus directly using the framing (AC1J1, DC1J1) and SPE indication signals (APL, DPL) to demultiplex the VT1.5s within the payload. Selection pins on these devices are used by the VT1.5 mappers to determine which VT1.5 payloads to handle. One OMar on each SPE is designated the master and determines and distributes SPE framing information in the transmit direction.

SLIF-S S-link interface

Before presentation to the STS mapping and DS1/VT termination section, the telecom bus is split into three 6.48 MHz buses, each representing a single STS-1 in the STS-3 envelope. This improves signal fan-out and lowers power usage and electromagnetic emissions.

Computing platform

The local processor on the NTLX71BA OC3 interface module contains four built-in serial communication controllers, DRAM, interfaces, timers, direct memory access controllers, and four Mbytes of flash electrically-erasable, programmable ROM and DRAM are provided.

Signaling

The following table shows the NTLX71BA OC3 interface module connector J1 (1SU) - power pinouts.

Pin number	A	B	C	D	E
2	-48B	-48B	-48B	-48B	-48B
3	NC	NC	NC	NC	NC
4	NC	NC	NC	NC	NC
5	RTN	RTN	RTN	RTN	RTN
6	NC	NC	NC	NC	NC
7	NC	NC	NC	NC	NC
8	-48A	-48A	-48A	-48A	-48A

The following table shows the NTLX71BA OC3 interface module connector J2 (2SU) - resource module (RM) common pinouts.

(Sheet 1 of 2)

Pin number	A	B	C	D	E
2	SYNC_ToCEM0	LGND	LGND	LGND	SYNC_FrOC30
3	SYNC_ToCEM1	.NC.	LGND	.NC.	SYNC_FrOC31
4	LGND	LGND	LGND	LGND	LGND
5	.NC.	.NC.	LGND	.NC.	.NC.
6	.NC.	.NC.	LGND	.NC.	.NC.
7	ToCEM0_D2	ToCEM0_D1	LGND	ToCEM1_D1	ToCEM1_D2
8	ToCEM0_D3	ToCEM0_CK	LGND	ToCEM1_CK	ToCEM1_D3
9	FrCEM0_D2	FrCEM0_D1	LGND	FrCEM1_D1	FrCEM1_D2
10	FrCEM0_D3	FrCEM0_CK	LGND	FrCEM1_CK	FrCEM1_D3
11	LGND	LGND	LGND	LGND	LGND

NTLX71BA OC3 interface module (continued)

(Sheet 2 of 2)

Pin number	A	B	C	D	E
12	.NC.	.NC.	LGND	.NC.	.NC.
13	.NC.	.NC.	LGND	.NC.	.NC.
14	.NC.	.NC.	LGND	.NC.	.NC.
15	.NC.	.NC.	LGND	.NC.	.NC.
16	SLOT_ID4	SLOT_ID3	MCTL	SLOT_ID1	SLOT_ID0
17	LGND	MPR	SLOT_ID2	MCLK	LGND
18	MMD	LGND	LGND	LGND	MSD

The following table shows the NTLX71BA OC3 interface module connector J2 (2SU) - extra S-link pinouts.

(Sheet 1 of 2)

Pin number	A	B	C	D	E
2	LGND	LGND	LGND	LGND	LGND
3	.NC.	.NC.	LGND	.NC.	.NC.
4	.NC.	.NC.	LGND	.NC.	.NC.
5	.NC.	.NC.	LGND	.NC.	.NC.
6	LGND	LGND	LGND	LGND	LGND
7	LGND	LGND	LGND	LGND	LGND
8	LGND	LGND	LGND	LGND	LGND
9	ToCEM0_D8	ToCEM0_D7	LGND	ToCEM1_D7	ToCEM1_D8
10	ToCEM0_D9	ToCEM0_CK3	LGND	ToCEM1_CK3	ToCEM1_D9
11	FrCEM0_D8	FrCEM0_D7	LGND	FrCEM1_D7	FrCEM1_D8
12	FrCEM0_D9	FrCEM0_CK3	LGND	FrCEM1_CK3	FrCEM1_D9
13	LGND	LGND	LGND	LGND	LGND

(Sheet 2 of 2)

Pin number	A	B	C	D	E
14	ToCEM0_D5	ToCEM0_D4	LGND	ToCEM1_D4	ToCEM1_D5
15	ToCEM0_D6	ToCEM0_CK2	LGND	ToCEM1_CK2	ToCEM1_D6
16	FrCEM0_D5	FrCEM0_D4	LGND	FrCEM1_D4	FrCEM1_D5
17	FrCEM0_D6	FrCEM0_CK2	LGND	FrCEM1_CK2	FrCEM1_D6
18	LGND	LGND	LGND	LGND	LGND

The following table shows the J4 OC-2 RM cross connector.

(Sheet 1 of 2)

Pin number	A	B	C	D	E
2	LGND	LGND	LGND	LGND	LGND
3	Drop0Data0	Drop0Data1	Add0Data2	Add0Data1	Add0Data0
4	Drop0Data3	Drop0Data4	Drop0Data2	Add0Data4	Add0Data3
5	Drop0Data5	Drop0Data6	LGND	Add0Data6	Add0Data5
6	Drop0Data7	DropSPE	LGND	Add0SPE	Add0Data7
7	Drop0C1J1V1	Drop0CLK	LGND	Add0CLK	Add0C1J1V1
8	Drop0Parity	LGND	LGND	LGND	Add0Parity
9	LGND	.NC.	LGND	.NC.	LGND
10	.NC.	.NC.	.NC.	.NC.	.NC.
11	.NC.	.NC.	.NC.	.NC.	.NC.
12	.NC.	.NC.	LGND	.NC.	.NC.
13	.NC.	.NC.	LGND	.NC.	.NC.
14	.NC.	.NC.	LGND	.NC.	.NC.
15	LGND	LGND	LGND	LGND	LGND
16	SpTx0	SpTx1	LGND	SpRx1	SpRx0

NTLX71BA OC3 interface module (continued)

(Sheet 2 of 2)

Pin number	A	B	C	D	E
17	SpTx2	SpTx3	LGND	SpRx3	SpRx2
18	LGND	LGND	LGND	LGND	LGND

The following table shows the NTLX71BA OC3 interface module backplane pin descriptions.

(Sheet 1 of 2)

Connection number	Signal	Function	IO type	Description
J1	-48B	power		-48 V battery feed B
J1	RET	power		Battery return
J1	-48A	power		-48 V battery feed A
J2	FrCEMnCKm	input	3.3 V CMOSSLIF-S	S-link clock lines from common equipment (n = 0 CEM0, n = 1 CEM1)
J2	FrCEMnDm	input	3.3 V CMOSSLIF-S	S-link data lines from common equipment (n = 0 CEM0,n = 1 CEM1)
J2	ToCEMnCKm	output	3.3 V CMOSSLIF-S	S-link clock lines to common equipment (n = 0 CEM0,n = 1 CEM1)
J2	ToCEMnDm	output	3.3 V CMOSSLIF-S	S-link data lines to common equipment (n = 0 CEM0,n = 1 CEM1) n = 1, 2, 3 on J2
J2	SYNC_ToCEM0 SYNC_ToCEM0 SYNC_FrOC3SYNC_FrOC3	output	3.3 V TTL74LVT16244	OC3 recovered frame pulse, used by CEM, or clock RM for synchronization
J2	MMD	input	3.3 V CMOSITM	JTAG 1149.5 bus master data
J2	MSD	input/output open drain	3.3 V CMOSITM	JTAG 1149.5 bus slave data

NTLX71BA OC3 interface module (continued)

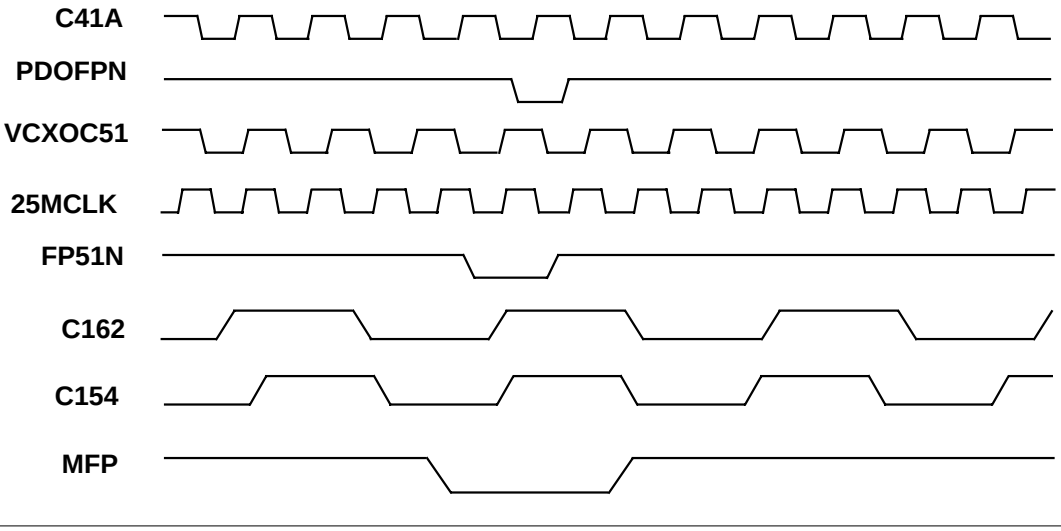
(Sheet 2 of 2)

Connection number	Signal	Function	IO type	Description
J2	MCLK	input	3.3 V CMOSITM	JTAG 1149.5 bus clock
J2	MPR	input/outputo pen drain	3.3 V CMOSITM	JTAG 1149.5 bus request
J2	MCTL	input	3.3 V CMOSITM	JTAG 1149.5 bus control
J2	LGND	power		logic ground of the PCP/BACKPLANE
J3	FrCEMnCKm	input	3.3 V CMOSSLIF-S	S-link clock lines from common equipment (n = 0 CEM0, n = 1 CEM1) m = 2, 3 on J3
J3	FrCEMnDm	input	3.3 V CMOSSLIF-S	S-link data lines from common equipment (n = 0 CEM0,n = 1 CEM1) n = 4, 5, 6, 7, 8, 9 on J2
J3	ToCEMnCKm	output	3.3 V CMOSSLIF-S	S-link clock lines to common equipment (n = 0 CEM0,n = 1 CEM1) m = 2, 3 on J3
J3	ToCEMnDm	output	3.3 V CMOSSLIF-S	S-link data lines to common equipment (n = 0 CEM0,n = 1 CEM1) n = 4, 5, 6, 7, 8, 9 on J2
J3	LGND	power	3.3 V CMOSSLIF-S	Logic ground of the PCP/BACKPLANE
J4	Drop0DatanDrop0C1J1Drop0PLDrop0PAR	output	3.3 V TTL74LVT16244	Enter OC3 resource module telecom bus DropODatan ranges from n = 0 to n = 7
J4	Add0DatanAdd0C1J1Add0PLAdd0PAR	input	3.3 V TTL74LVT16244	Enter OC3 resource module telecom bus Add0Datan ranges from n = 0 to n = 7
J4	LGND	power		Logic ground of the PCP/BACKPLANE

NTLX71BA OC3 interface module (end)

Timing

The following figure shows the clock phase relationships for the NTLX71BA OC3 interface module.



Legend:
C41A — 24.576 MHz system clock derived from the active CEM
PDOFPN — Transmit frame indication derived from the active CEM
VCXOC51 — 19.44 MHz SONET transmit clock synthesized from C41A and PDOFPN
25MCLK — 25.92 MHz SONET clock, used by OMaR devices (synthesized from VCX0C51 and FP15N)
FP51N — Frame pulse based on the 19.44 MHz synthesized clock (VCXOC51)
C162 — Transmit DS-1 clock used by OMaR devices, derived from VCXOC51 and FP51N
C154 — STS-1 rate telecom bus clock derived from VCXO51 and FP51N
MFP — Master frame pulse based on the C154 clock

Power requirements

The following table shows the NTLX71BA OC3 interface module general power requirements.

Parameter	Minimum	Maximum	Units
Supply voltage	39.0	053.0	V
Supply noise		100.0	mV
Supply current		001.0	A

NTLX72AA DLC

Description

The NTLX72AA data link controller (DLC) resource module (RM) provides resources for call processing for the DMS-Spectrum Peripheral Module (SPM).

ATTENTION

The data link controller (DLC) may not apply to all markets.

Location

The NTLX72AA DLC RM optionally occupies slots 1 and 7 on shelf 1 of the dual-shelf assembly. The quantities and locations of DLC RM are office dependent.

The DLC RM provides data-link layer protocol termination for multiple-port data communications using HDLC-based frame structures, such as LAPD for ISDN PRI. The DLC RM serves as a bridge between external link layer protocols based on HDLC and a proprietary DMS internal messaging protocol, DMSW.

The hardware architecture of the new resource module is flexible and expandable such that it can accommodate future HDLC-based applications with minimal changes/additions.

Function

The principal functions of the DLC RM are:

- termination of layer 2 HDLC protocol messages
- termination of proprietary (DMSW) data link protocol messages to and from the active and the inactive CEM
- protocol conversion between HDLC frames and DMSW messages for layer 3 data to be processed within the SPM or DMS core (such as call control information)
- statistical multiplexing/demultiplexing and retransmission of HDLC frames for layer 3 data to be processed externally (such as user data packets)
- transmission and reception of layer 1 data to and from the CEMs using the SPM S-Link serial bus

NTLX72AA DLC (continued)

Features

The DLC RM provides the following features:

- support for the Q.921 LAPD protocol
- DS-0 (64 kb/s), sub-DS-0 (16 kb/s), and wideband (n*64 kb/s) data rates
- 100 MHz PowerPC 603e-based processing engine
- integrated test and maintenance support employing an IEEE 1149.1 compliant JTAG boundary scan master
- on-board point-of-use power supply (PUPS). Typical power useage is 21 watts, not to excees 25 watts.
- an expandable architecture which can support a range of HDLC terminations from 128 to 512 independent channels, in 128 channel increments. To minimize product cost, the initial hardware release only supports 128 channels, which is sufficient for the PRI application. The hardware design supports the maximum number of terminations, but only one HDLC controller device is installed.

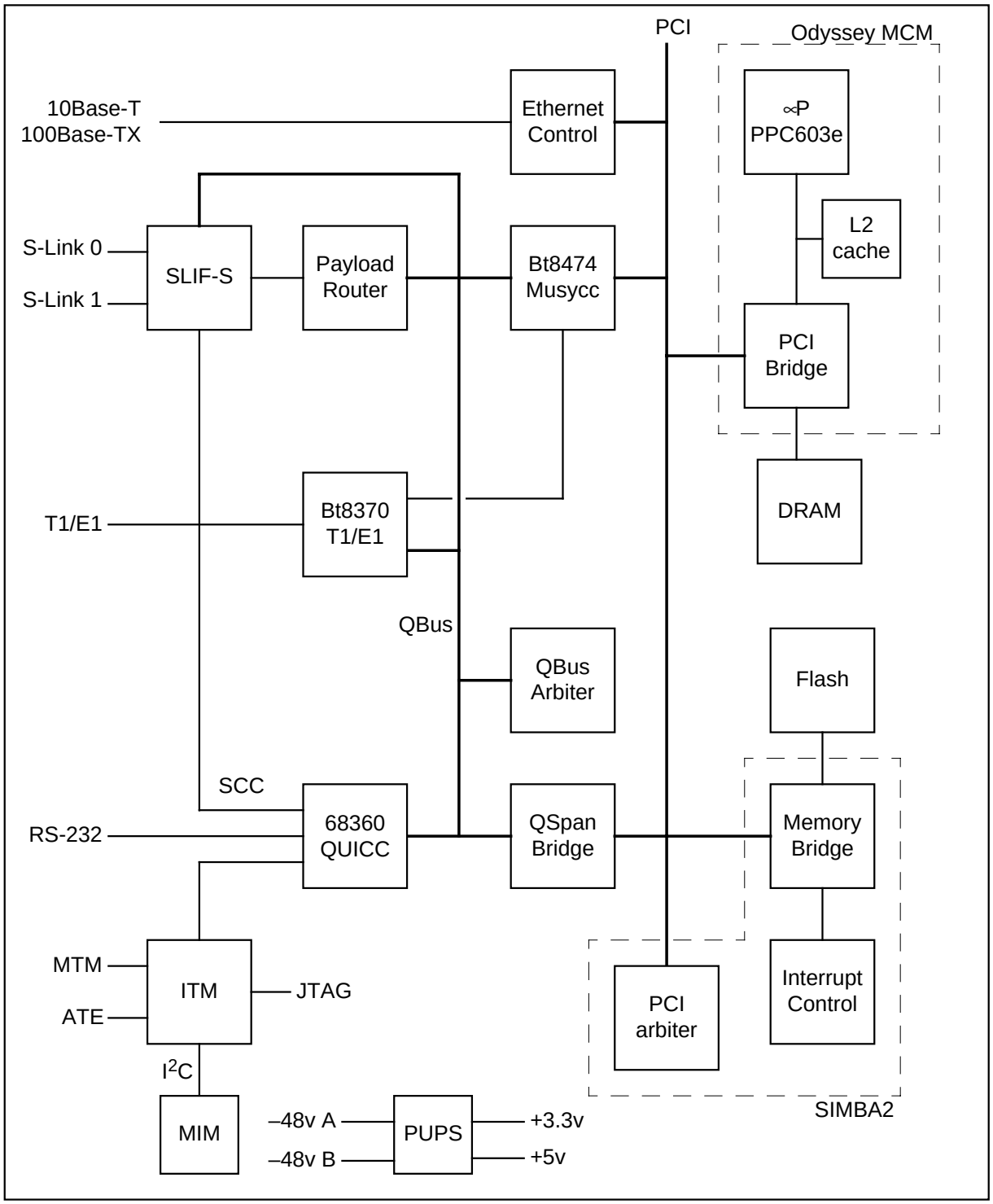
Functional blocks

The NTLX72AA DLC RM has the following functional blocks:

- S-link interface
- Payload router
- Multi-channel HDLC controllers
- Processor complex
- Quad integrated communications controller (QUICC)
- QSpan bridge
- PCI bus arbiter
- Interrupt controller
- Ethernet controller
- Integrated test bus master
- Power supply

The following figure represents the functional block diagram of the DLC RM.

NTLX72AA DLC (continued)



NTLX72AA DLC (continued)

S-link interface

A slave S-Link interface (SLIF-S), common to all RM types, is responsible for the physical interface. The SLIF-S performs the following functions:

- recovers data from the S-Links from both CEM modules
- monitors link health using CRC checks
- extracts the DMSW messaging channels from both CEM modules
- selects PCM data from the CEMs, based on CEM activity. A small elastic storage function accommodates phase variations between the CEMs.
- formats the selected data stream and places it onto an internal parallel bus for access by other resources within the RM
- broadcasts outgoing PCM data to both CEMs
- inserts outgoing DMSW messaging timeslots to each CEM
- calculates and inserts link CRC values
- provides facilities for low-level link, RM control, and RM status facilities, including test and ID storage

An S-Link connects the DLC RM to each of the two CEMs.

Payload router

The payload router converts between the multiplexed parallel PCM bus of the SLIF-S and the individual serial data streams of the HDLC controllers. Channel mapping is fixed in the payload router since DS0 switching is done in the CEMs and channel-to-port assignments are configurable within the HDLC controllers.

Multi-channel HDLC controllers

The generic HDLC layer 2 termination function is accomplished using a set of HDLC controller devices. The HDLC controllers provide the following Layer 2 communication functions:

- flag insertion/detection
- payload insertion/extraction
- zero-bit insertion/deletion for flag transparency
- CRC generation/checking
- error detection
- inter-frame idle insertion
- aborted message indication/detection

Serial time-division multiplexed buses send HDLC messages to and from the payload router. On the processor side, each HDLC controller has direct memory access (DMA) to a common host bus for retrieving and depositing the message payload in main memory. Internal buffering in both transmit and receive directions reduces the overhead in host bus utilization. Message data structure is controlled through a set of descriptors which are also stored in main memory.

Each HDLC controller manages up to 128 channels. The hardware architecture supports up to 4 controllers per module.

Processor complex

The processor complex, in conjunction with the HDLC controllers, performs all of the specific link layer protocol (for example, LAPD). The processor complex also is responsible for the local initialization, configuration, and maintenance of the resource module, as well as communication with the CEMs using the S-Link messaging facility.

A 100 MHz PowerPC 603e is integrated with a level 2 cache memory as well as a bus bridge and main memory controller. This uses the same field-proven multi-chip module found on the CEM.

A bank of DRAM memory provides program storage for the processor, message data buffer, and descriptor memory. Flash memory provides non-volatile storage of boot code and internal fault information, as well as an image of the application code.

Quad integrated communications controller (QUICC)

Several of the communication ports on the DLC are implemented using a Motorola 68360 Quad Integrated Communications Controller (QUICC) processor operating in the slave (CPU disabled) mode. A bus bridge adapts the QUICC's bus to the PCI bus for communication with the host processor. The QUICC provides the following functions required on the DLC:

- two serial communication controller (SCC) buses which transport data to and from the SLIF-S DMSW messaging block
- a serial peripheral interface (SPI) bus for ITM access
- a UART interface used for initial hardware and software debug
- chip select and write enable signals for Q-Bus peripherals
- watchdog and general purpose timers

NTLX72AA DLC (continued)

QSpan bridge

The QSpan Bridge adapts the PCI bus to the QUICC bus (QBus) which provides host processor access to the QUICC and QBus peripherals, and also allows the QUICC to access main memory using the PCI bus.

PCI bus arbiter

The bus arbiter receives requests for host bus access from the processor, HDLC controllers, QSpan bridge, and Ethernet controller. It grants access to one agent at a time, ensuring each agent has fair access to the bus.

Interrupt controller

The interrupt controller provides a consolidation point for all of the interrupt sources on the module. The interrupt controller presents one maskable and one non-maskable interrupt to the host processor.

Ethernet controller

A 10/100Base-T Ethernet interface is provided on the prototype circuit packs to aid in the design and debug of the module software. This circuitry is not present on production units for field use.

Integrated test bus master

The integrated test bus master (ITM) interfaces the system module test and maintenance (MTM) bus to the resource module, providing access to the internal JTAG bus, processor communication, circuit pack reset control, module information memory access, and circuit pack LED control.

Power supply

A DC-to-DC point-of-use power supply (PUPS) converts the -48V A and B feeds to the +3.3V and +5V supply rails required for the module circuitry.

Electromagnetic compatibility

The DLC resource module, when inserted into an SPM rack and operating to provide PRI service, does not cause the SPM to fail to meet the applicable electromagnetic compatibility (EMC), radio frequency immunity (RFI), or electrostatic discharge (ESD) requirements imposed by applicable regulatory and internal Nortel guidelines.

The physical packaging of the DLC RM provides EM shielding for the circuit pack and the integrated circuits (ICs) it contains. This shielding is part of the EMC strategy to meet emissions and immunity requirements. Apertures in the modules prevent leakage of high-frequency noise beyond the level provided in the EMC budget.

Although the module shielding reduces emissions from the circuit packs and ICs, it does not prevent noise conducted on attached cables. The modules are referenced to frame ground through a gasket to the multilayer backplane (with external ground layers) and through the guide pins in the backplane connector.

PRI synchronization requirements

The PRI application places no special synchronization requirements on the SPM equipment and continues to work regardless of the synchronization mode selected for the SPM.

NTLX82AA CEM

Product description

The NTLX82AA common equipment module (CEM) provides the centralized resources required to support DMS-Spectrum Peripheral Module (SPM) applications. The NTLX82AA CEM is a replacement for NTLX63AA CEM.

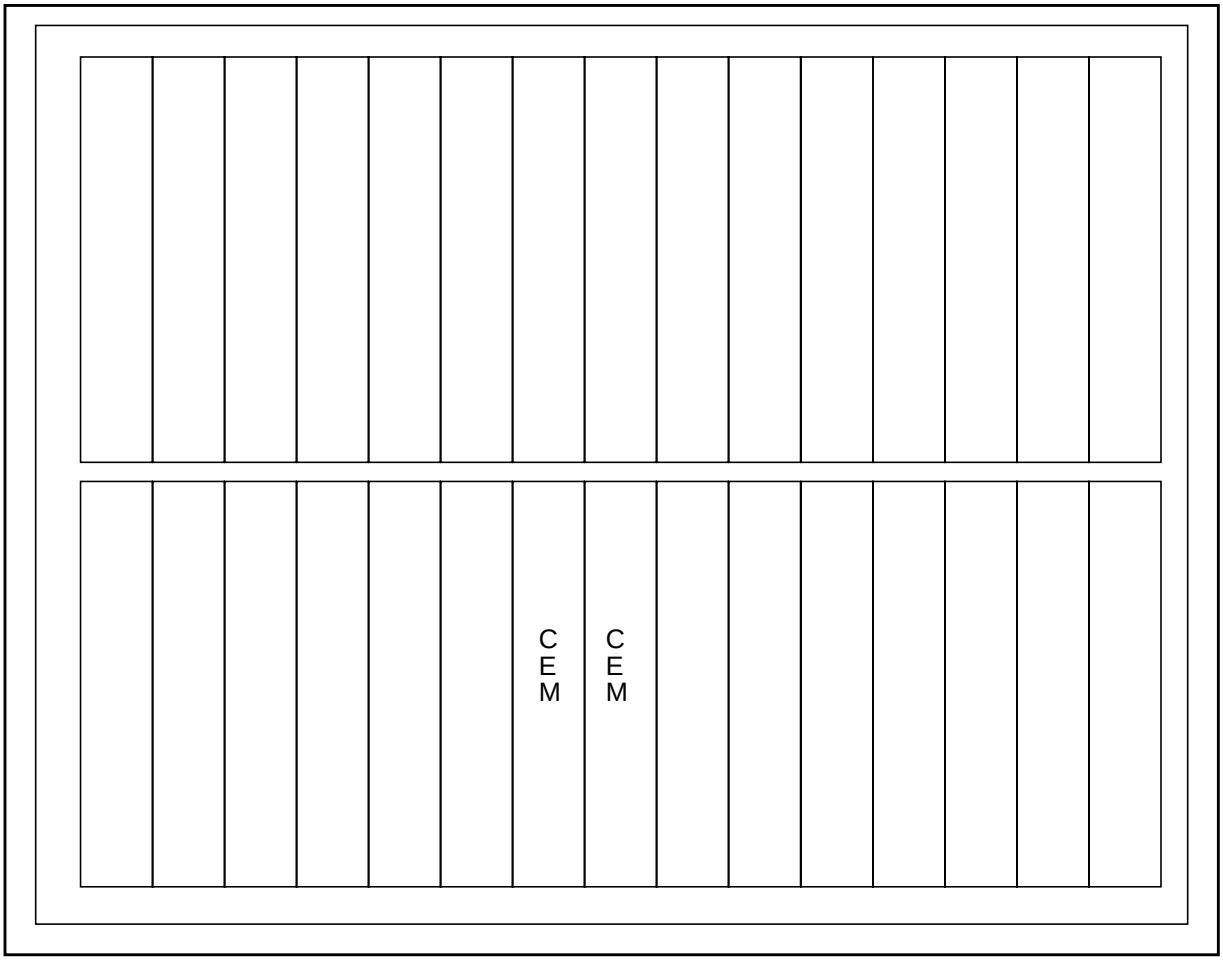
The following are the enhancements available when NTLX63AA CEM is upgraded to the NTLX82AA CEM:

- The Celestica Point of Use Power Supplies (PUPS) are replaced by Lucent PUPS.
- The CEM memory size is increased to 128 megabytes.
- The self-test diagnostics have improved power.
- The FLASH memory is increased to 96 megabytes.
- An Ethernet port on the faceplate is productized. This port is a software loading port for a standalone Succession Multi-Services Gateway (SMG) configuration.

Location

The two NTLX82AA CEMs are located in slots 7 and 8 on shelf 0 of the NTLX51AA or BA dual-shelf assembly.

SPM Shelf with two CEM cards



Functional description

The NTLX82AA CEM pair provides the following functions:

- bandwidth allocation
- communication and messaging
- computing platform
- network synchronization and timing subsystem
- 1 + 1 redundancy

NTLX82AA CEM (continued)

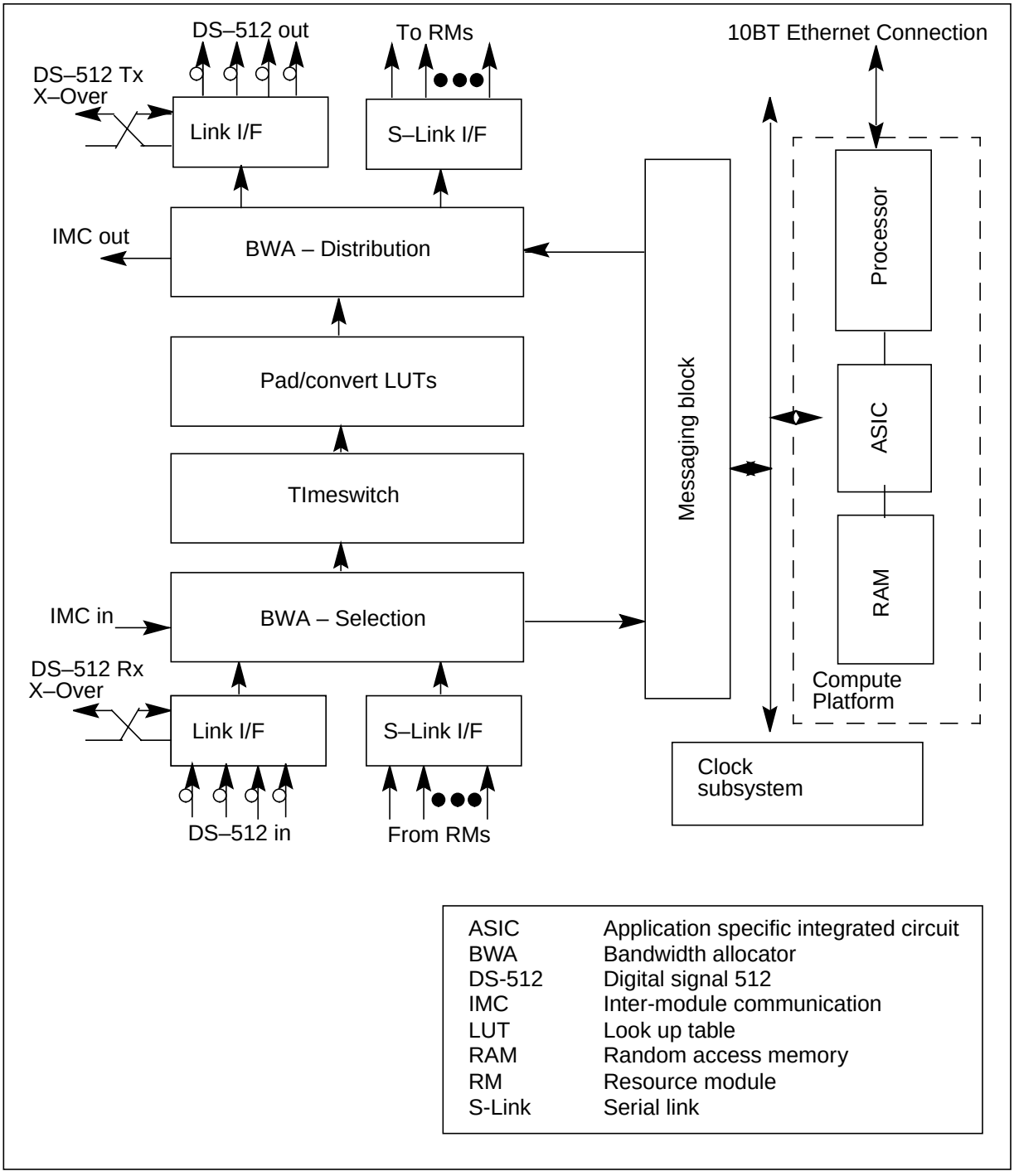
Functional blocks

NTLX82AA CEM has the following functional blocks:

- DS-512 link interface
- S-Link interface
- bandwidth allocator
- timeswitch
- pad/convert LUTs
- messaging block
- compute platform
- clock subsystem

NTLX82AA CEM (continued)

NTLX82AA CEM functional blocks



ASIC	Application specific integrated circuit
BWA	Bandwidth allocator
DS-512	Digital signal 512
IMC	Inter-module communication
LUT	Look up table
RAM	Random access memory
RM	Resource module
S-Link	Serial link

NTLX82AA CEM (continued)

DS-512 Link Interface

The DS-512 interface is shown in two parts, receive and transmit. When receiving, this block is responsible for:

- recovering the data and frame from the DS-512 link, including O/E and 12B10B conversion
- monitoring link status
- performing slip buffering, to enable the operation in the presence of a synchronization fault between the SPM and the network
- performing crossover of received data with the other CEM by means of the Rx crossover bus
- accommodating (small) phase differences between the two CEMs using elastic stores
- extracting the message channel (separate from PCM to reduce delay, and thus improve messaging performance)
- extracting and detecting the channel supervisory message (CSM) on both planes
- selecting the plane of PCM channels between the enhanced network (ENET) planes, on a per DS-0 basis

When transmitting, this block is responsible for:

- combining host messaging timeslots with those of the mate CEM (when required)
- inserting CSM data
- accepting PCM timeslots from the active CEM by means of the Tx crossover bus, when this CEM is inactive
- performing the 10B12B conversion, inserting the framing channel and performing E/O conversion
- generating the link transmit clock, phase locked to the active CEM system clock (this enables operation of these links, even if the system clock on this CEM is inoperative

Physically, this block is implemented with the following two ASICs:

- quad link controller (QLC)
- CSM & plane select device

S-Link Interface

The S-Link interface is shown in two parts: receive and transmit. This block is responsible for converting the parallel data format used on the CEM and the

256 timeslot serial links to interface with the resource modules. In addition, it distributes the system clock to the resource modules, and provides low level control and status by means of overhead bits embedded in the S-Link format.

Physically, this block is composed of 6 identical S-Link interface master devices (SLIF-M), each processing 16 S-Links.

Bandwidth Allocator

The bandwidth allocator (BWA) function is shown in two parts, selection (BWA-S) and distribution (BSWA-D). This block operates much like a double buffered timeswitch, except it cycles over 32 times per frame. Thus, it has a connection resolution of 128 timeslots, and an average through delay (each side) of 1/32 frame. Each set of 32 timeslots is referred to as a bandwidth allocator group. Each component (BWA-S and BWA-D) is capable of broadcast connections.

The BWA is an asymmetrical matrix, with 26K timeslots (768 P-side & 64 C-side BWA groups) on the S-Link side, and 12K timeslots (384 BWA groups) on the timeswitch side.

This block is used to:

- groom platform overhead timeslots from the S-Links to the timeswitch, and vice-versa, allowing for variations in timeslot usage by various RMs
- merge selectively the C-side timeslot stream with those from the S-Links
- apply digital padding (selectable on a per-DS-0 basis) to timeslots from the timeswitch
- extract and insert messaging channels from the timeslot stream, and present them to the messaging block
- assist in RM sparing, by providing a mechanism by which traffic can be rapidly switched between RMs

Timeswitch

The timeswitch provides single timeslot rearrangement functions. It has 12K timeslots, and is a double buffered (N x DS-0 capable) design, based on ENET components. The timeswitch receives input from the BWA and acts as a matrix. Together with the BWA, it maps the C-side DS-512 channels to P-side channels on the SPM backplane. Those P-side channels connect to RMs. Therefore the timeswitch is a key component in mapping DS-0 connections from the ENET to the RMs that transport signals like the OC3 or ATM RM.

NTLX82AA CEM (continued)

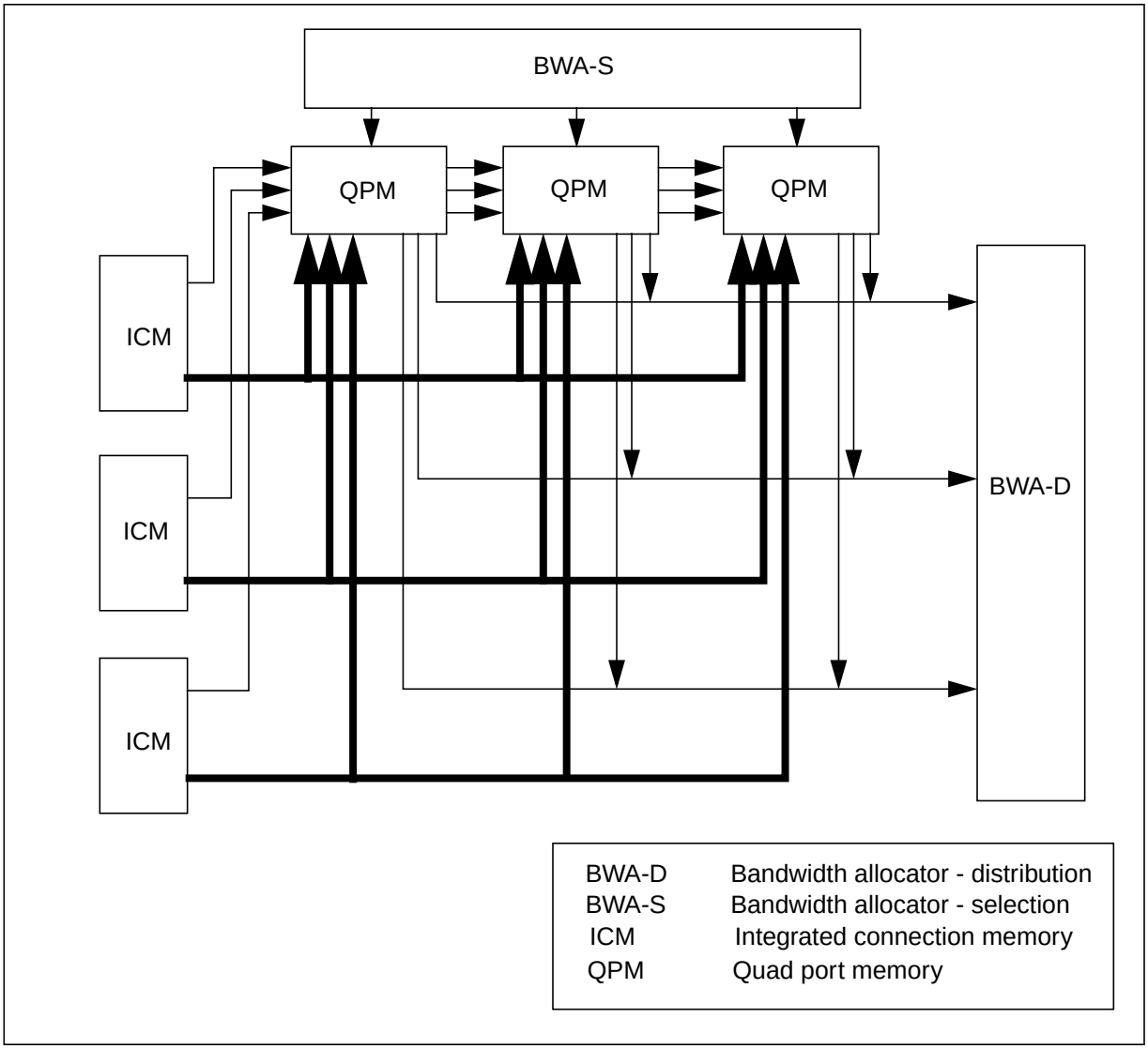
Physically, it is composed of six devices:

- three quad port memory (QPM) ASICs
- three integrated connection memory (ICM) ASICs

The following figure illustrates how the timeswitch does the following.

- receives input from the bandwidth allocator - selection (BWA-S)
- integrated connection memory (ICM) maps the input and output ports on the quad port memory (QPM) to the bandwidth allocator - distribution (BWA-D)
- QPM chips transfer data from BWA-S to the BWA-D

Timeswitch functional illustration



Pad/convert LUTs

The padding look up tables (LUTs) module provides a generalized PCM conversion facility, normally used to implement gain and loss padding as required for the gain/loss plan. It provides up to 16 conversion tables, selectable on a per-DS-0 basis for the 12K timeslot stream from the timeswitch. Table selection is provided by means of bits from the ICM ASICs used to control the timeswitch. It is implemented as a function of the BWA ASIC in distribution mode.

NTLX82AA CEM (continued)

Messaging block

This block provides DMS protocol messaging functionality. Up to 32 messaging ports can be provisioned. Each port is capable of N x DS-0 bandwidth. Each port can be provisioned to use one of the following protocols:

- DMS-Y for messaging to the message switch (MS) and core
- DMS-W for messaging internal to the SPM

The messaging ports are used for host messaging (4 ports), RM messaging (26 ports), IMC messaging (1 port), and 1 spare port for diagnostics.

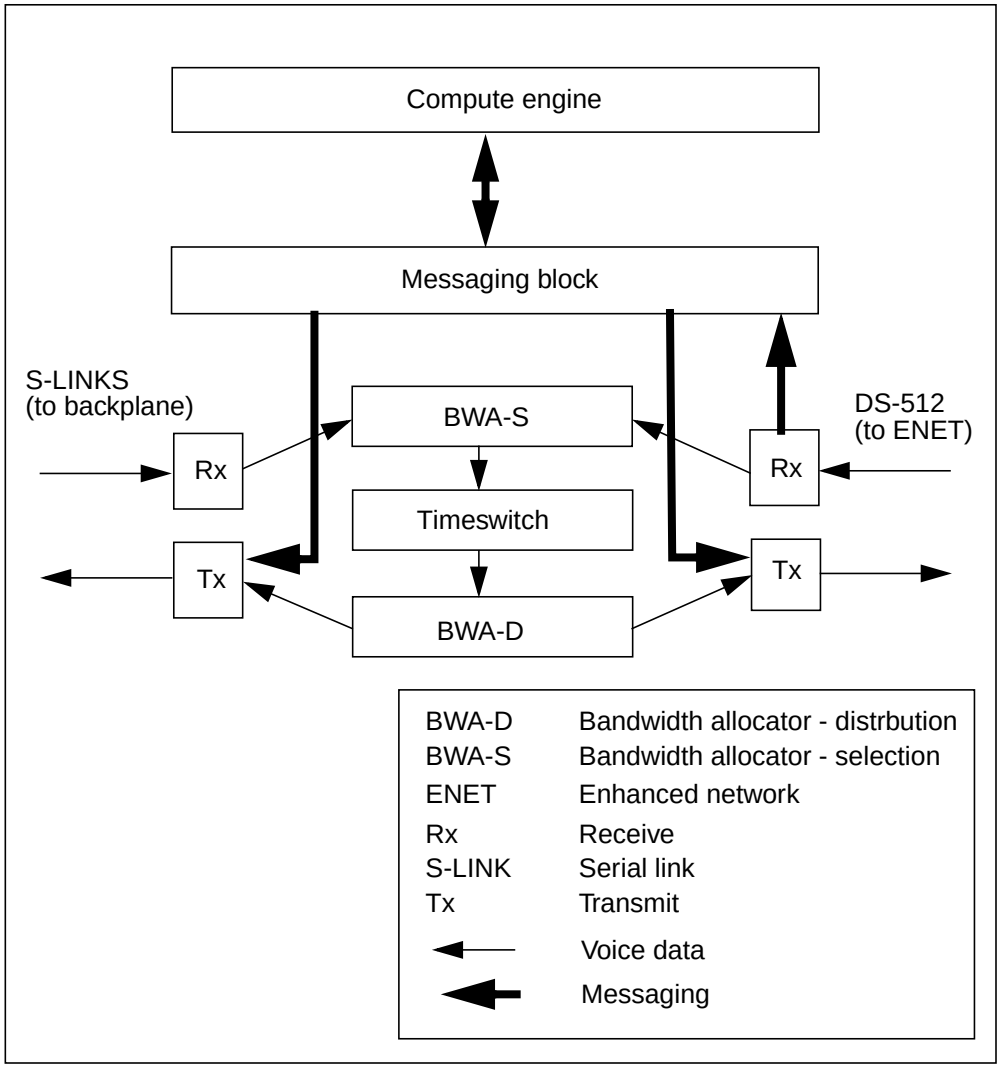
This block can terminate messages by DMA access into the processor memory.

Physically it is composed of

- one link protocol messaging interface controller (LPMIC) ASIC
- one integrated connection memory (ICM)

The following figure indicates how the messaging block relates to the compute engine, the DS-512 transmit and receive interfaces, and the bandwidth allocator blocks. Through the bandwidth allocator - distribution (BWA-D), the messaging block communicates with the resource modules (RM) in the SPM.

Messaging block functional diagram



Compute Platform

The CEM main processor is implemented with a multi-chip module (MCM) processor block. It has 128 MB of 66 MHz EDO RAM and 96 MB Flash as well as 10BT Ethernet connection

Clock Subsystem

This clock is responsible for generating the SPM system clock. It can generate a clock phase locked (8 KHz) to either plane of the network by means of a DS-512 link, or phase information acquired from a RM slot. It is implemented with a small microprocessor (68307), digital to analog converter, and the TIC ASIC. This block also determines common equipment module activity and

NTLX82AA CEM (continued)

coordinates SWitch of ACTivity (SWACT). The clock from this subsystem is distributed to the RMs by means of the S-Links.

Miscellaneous

In addition to the above, the CEM contains support for test functions (JTAG) provided by an integrated testbus master (ITM) ASIC, and alarm and visual indicator LED control.

Signaling

The following table shows NTLX82AA CEM backplane connections.

(Sheet 1 of 7)

Pin	A	B	C	D	E
2	LGND	LGND	LGND	LGND	LGND
3	ToCEM_ SLOT22D2	ToCEM_ SLOT22D1	LGND	ToCEM_ SLOT23D2	ToCEM_ SLOT23D2
4	ToCEM_ SLOT22D3	ToCEM_ SLOT22CK	LGND	ToCEM_ SLOT23CK	ToCEM_ SLOT23D3
5	FrCEM_ SLOT22D2	FrCEM_ SLOT22D1	LGND	FrCEM_ SLOT23D1	FrCEM_ SLOT23D2
6	FrCEM_ SLOT22D3	FrCEM_ SLOT22CK	LGND	FrCEM_ SLOT23CK	FrCEM_ SLOT23D3
7	ToCEM_ SLOT21D2	ToCEM_ SLOT21D1	LGND	ToCEM_ SLOT24D1	ToCEM_ SLOT24D2
8	ToCEM_ SLOT21D3	ToCEM_ SLOT21CK	LGND	ToCEM_ SLOT24CK	ToCEM_ SLOT24D3
9	FrCEM_ SLOT21D2	FrCEM_ SLOT21D1	LGND	FrCEM_ SLOT24D1	FrCEM_ SLOT24D2
10	FrCEM_ SLOT21D3	FrCEM_ SLOT21CK	LGND	FrCEM_ SLOT24CK	FrCEM_ SLOT24D3
11	LGND	LGND	LGND	ToCEM_ SLOT25D1	ToCEM_ SLOT25D2
12	ToCEM_ SLOT20D2	ToCEM_ SLOT20D1	LGND	ToCEM_ SLOT25CK	ToCEM_ SLOT25D3

NTLX82AA CEM (continued)

(Sheet 2 of 7)

13	ToCEM_ SLOT20D3	ToCEM_ SLOT20CK	LGND	FrCEM_ SLOT25D1	FrCEM_ SLOT25d2
14	FrCEM_ SLOT20D2	FrCEM_ SLOT20D1	LGND	FrCEM_ SLOT25CK	FrCEM_ SLOT25D3
15	FrCEM_ SLOT20D3	FrCEM_ SLOT20CK	LGND	LGND	LGND
16	ToCEM_ SLOT19D2	ToCEM_ SLOT19D1	LGND	ToCEM_ SLOT26D1	ToCEM_ SLOT26D2
17	ToCEM_ SLOT19D3	ToCEM_ SLOT19CK	LGND	ToCEM_ SLOT26CK	ToCEM_ SLOT26D3
18	ToCEM_ SLOT19D2	FrCEM_ SLOT19D1	LGND	FrCEM_ SLOT26D1	FrCEM_ SLOT26D2
19	FrCEM_ SLOT19D3	FrCEM_ SLOT19CK	LGND	FrCEM_ SLOT26CK	FrCEM_ SLOT26D3
20	ToCEM_ Sp17D	ToCEM_ Sp17CK	LGND	ToCEM_ SLOT27D1	ToCEM_ SLOT27D2
21	FrCEM_ Sp17D	FrCEM_ Sp17CK	LGND	ToCEM_ SLOT27CK	ToCEM_ SLOT27D3
22	LGND	LGND	LGND	FrCEM_ SLOT27D1	FrCEM_ SLOT27D2
23	ToCEM_ SLOT18D2	ToCEM_ SLOT18D1	LGND	FrCEM_ SLOT27CK	FrCEM_ SLOT27D3
24	ToCEM_ SLOT18D3	ToCEM_ SLOT18D2	LGND	ToCEM_ SLOT28D1	ToCEM_ SLOT28D2
25	FrCEM_ SLOT18D2	FrCEM_ SLOT18D1	LGND	ToCEM_ SLOT28CK	ToCEM_ SLOT28D3
26	FrCEM_ SLOT18D3	FrCEM_ SLOT18CK	LGND	FrCEM_ SLOT28D1	FrCEM_ SLOT28D2
27	ToCEM_ SLOT17D2	ToCEM_ SLOT17D1	LGND	FrCEM_ SLOT28CK	FrCEM_ SLOT28D3
28	ToCEM_ SLOT17D3	ToCEM_ SLOT17CK	LGND	LGND	LGND

NTLX82AA CEM (continued)

(Sheet 3 of 7)

29	FrCEM_ SLOT17D2	FrCEM_ SLOT17D1	LGND	ToCEM_ SLOT14D1	ToCEM_ SLOT14D2
30	FrCEM_ SLOT17D3	FrCEM_ SLOT17CK	LGND	ToCEM_ SLOT14CK	ToCEM_ SLOT14D3
31	ToCEM_ SLOT16D2	ToCEM_ SLOT16D1	LGND	FrCEM_ SLOT14D1	FrCEM_ SLOT14D3
32	ToCEM_ SLOT16D3	ToCEM_ SLOT16CK	LGND	FrCEM_ SLOT14CK	FrCEM_ SLOT14D3
33	FrCEM_ SLOT16D2	FrCEM_ SLOT16D1	LGND	ToCEM_ SLOT13D1	ToCEM_ SLOT13D2
34	FrCEM_ SLOT16D3	FrCEM_ SLOT16CK	LGND	ToCEM_ SLOT13CK	ToCEM_ SLOT13D3
35	ToCEM_ Sp15D	ToCEM_ Sp15CK	LGND	FrCEM_ SLOT13D1	FrCEM_ SLOT13D2
36	FrCEM_ Sp15D	FrCEM_ Sp15CK	LGND	FrCEM_ SLOT13CK	FrCEM_ SLOT13D3
37	ToMATE_ QLC	FrMATE_ QLC	LGND	LGND	LGND
38	ToMATE_ RXPCM0	ToMATE_ RXPCM1	LGND	FrMATE_ RXPCM1	FrMATE_ RXPCM0
39					
40	ToMATE_ RXPCM2	ToMATE_ RXPCM3	LGND	FrMATE_ RXPCM3	FrMATE_ RXPCM2
41	ToMATE_ RXPCM4	ToMATE_ RXPCM5	LGND	FrMATE_ RXPCM5	FrMATE_ RXPCM4
42	ToMATE_ RXPCM6	ToMATE_ RXPCM7	ToMATE_ RXPCM8	FrMATE_ RXPCM7	FrMATE_ RXPCM6
43	ToMATE_ RXPCM_FPN	ToMATE_ RXPCM9	FrMATE_ RXPCM8	FrMATE_ RXPCM9	FrMATE_ RXPCM_FPN
44	ToMATE_ CSIDE	ToMATE_ RXPCM_CLK	LGND	FrMATE_ RXPCM_CLK	FrMATE_ CSIDE
45	ToMATE_ TXPCM0	ToMATE_ DS1	LGND	FrMATE_ DS1	FrMATE_ TXPCM0

(Sheet 4 of 7)

46	ToMATE_ TXPCM2	ToMATE_ TXPCM1	LGND	FrMATE_ TXPCM1	FrMATE_ TXPCM2
47	ToMATE_ TXPCM4	ToMATE_ TXPCM3	LGND	FrMATE_ TXPCM3	FrMATE_ TXPCM4
48	ToMATE_ TXPCM7	ToMATE_ TXPCM5	ToMATE_ TXPCM6	FrMATE_ TXPCM5	FrMATE_ TXPCM7
49	ToMATE_ TXPCM9	ToMATE_ TXPCM8	FrMATE_ TXPCM6	FrMATE_ TXPCM8	FrMATE_ TXPCM9
50	ToMATE_ TXPCM_FPN	ToMATE_ TXPCM10	LGND	FrMATE_ TXPCM10	FrMATE_ TXPCM_FPN
51	ToMATE_ IMC0	ToMATE_ TXPCM_CLK	LGND	FrMATE_ TXPCM_CLK	FrMATE_ IMC0
52	ToMATE_ IMC2	ToMATE_ IMC1	LGND	FrMATE_ IMC1	FrMATE_ IMC2
53	ToMATE_ IMC4	ToMATE_ IMC3	LGND	FrMATE_ IMC3	FrMATE_ IMC4
54	ToMATE_ IMC_FPN	ToMATE_ IMC_CLK	ToMATE_ ACT	FrMATE_ IMC_CLK	FrMATE_ IMC_FPN
55	ToMATE_ SFPN	ToMATE_ PRES	FrMATE_ ACT	FrMATE_ PRES	FrMATE_ SFPN
56	ToMATE_ RSTREQ	ToMATE_ TOD	ToMATE_ ACTDROP	FrMATE_ TOD	FrMATE_ RSTREQ
57	ToMATE_ SYS_FPN	ToMATE_ SYS_CLK	FrMATE_ ACTDROP	FrMATE_ SYS_CLK	FrMATE_ SYS_FPN
58	LGND	LGND	ToMATE_ FAIL	LGND	LGND
59	ToCEM_ SLOT15D2	ToCEM_ SLOT15D1	FrMATE_ FAIL	ToCEM_ SLOT12D1	ToCEM_ SLOT12D2
60	ToCEM_ SLOT15D3	ToCEM_ SLOT15CK	LGND	ToCEM_ SLOT12CK	ToCEM_ SLOT12D3
61			LGND		
62	FrCEM_ SLOT15D2	FrCEM_ SLOT15D1	LGND	FrCEM_ SLOT12D1	FrCEM_ SLOT12D2
63	FrCEM_ SLOT15D3	FrCEM_ SLOT15CK	LGND	FrCEM_ SLOT12CK	FrCEM_ SLOT12D3

NTLX82AA CEM (continued)

(Sheet 5 of 7)

64	ToCEM_ Sp1D	ToCEM_ Sp1CK	LGND	ToCEM_ SLOT11D1	ToCEM_ SLOT11D2
65	FrCEM_ Sp1D	FrCEM_ Sp1CK	LGND	FrCEM_ SLOT11CK	FrCEM_ SLOT11D3
66	ToCEM_ SLOT1D2	ToCEM_ SLOT1D1	LGND	FrCEM_ SLOT11D1	FrCEM_ SLOT11D2
67	ToCEM_ SLOT1D3	ToCEM_ SLOT1CK	LGND	FrCEM_ SLOT11CK	FrCEM_ SLOT11D3
68	FrCEM_ SLOT1D2	FrCEM_ SLOT1D1	LGND	LGND	LGND
69	FrCEM_ SLOT1D3	FrCEM_ SLOT1CK	SYNC_FrSRMO	ToCEM_ SLOT10D7	ToCEM_ SLOT10D8
70	ToCEM_ SLOT2D2	ToCEM_ SLOT2D1	LGND	ToCEM_ SLOT10CK3	ToCEM_ SLOT10D9
71	ToCEM_ SLOT2D3	ToCEM_ SLOT2CK	LGND	FrCEM_ SLOT10D7	FrCEM_ SLOT10D8
72	FrCEM_ SLOT2D2	FrCEM_ SLOT2D1	LGND	FrCEM_ SLOT10CK3	FrCEM_ SLOT10D9
73	FrCEM_ SLOT2D3	FrCEM_ SLOT2CK	LGND	ToCEM_ SLOT10D4	FrCEM_ SLOT10D5
74	LGND	LGND	LGND	ToCEM_ SLOT10CK2	ToCEM_ SLOT10D6
75	ToCEM_ Sp3D	ToCEM_ Sp3CK	SYNC_FrOC3_ 1	FrCEM_ SLOT10D4	FrCEM_ SLOT10D5
76	FrCEM_ Sp3D	FrCEM_ Sp3CK	LGND	FrCEM_ SLOT10CK2	FrCEM_ SLOT10D6
77	ToCEM_ SLOT3D2	ToCEM_ SLOT3D1	LGND	ToCEM_ SLOT10D1	ToCEM_ SLOT10D2
78	ToCEM_ SLOT3D3	ToCEM_ SLOT3CK	SYNC_FrSRM_ 1	ToCEM_ SLOT10CK1	ToCEM_ SLOT10D3
79	FrCEM_ SLOT3D2	FrCEM_ SLOT3D1	LGND	FrCEM_ SLOT10D1	FrCEM_ SLOT10D2

(Sheet 6 of 7)

80	FrCEM_ SLOT3D3	FrCEM_ SLOT3CK	LGND	FrCEM_ SLOT10CK1	FrCEM_ SLOT10D3
81	ToCEM_ SLOT4D2	ToCEM_ SLOT4D1	LGND	LGND	LGND
82	ToCEM_ SLOT4D3	ToCEM_ SLOT4CK	CEM_SLOT_ID	ToCEM_ SLOT9D7	ToCEM_ SLOT9D8
83	FrCEM_ SLOT4D2	FrCEM_ SLOT4D1	LGND	ToCEM_ SLOT9CK3	ToCEM_ SLOT9D9
84	FrCEM_ SLOT4D3	FrCEM_ SLOT4CK	BKPLN_ID3	FrCEM_ SLOT9D7	FrCEM_ SLOT9D8
85	LGND	LGND	LGND	FrCEM_ SLOT9CK3	FrCEM_ SLOT9D8
86	ToCEM_ SLOT5D2	ToCEM_ SLOT5D1	SYNC_FrOC3_ 0	ToCEM_ SLOT9D4	ToCEM_ SLOT9D5
87	ToCEM_ SLOT5D3	ToCEM_ SLOT5CK	LGND	ToCEM_ SLOT9CK2	ToCEM_ SLOT9D6
88	FrCEM_ SLOT5D2	FrCEM_ SLOT5D1	BKPLN_ID2	FrCEM_ SLOT9D4	FrCEM_ SLOT9D5
89	FrCEM_ SLOT5D3	FrCEM_ SLOT5CK	LGND	FrCEM_ SLOT9CK2	FrCEM_ SLOT9D6
90	ToCEM_ SLOT6D2	ToCEM_ SLOT6D1	BKPLN_ID1	ToCEM_ SLOT9D1	ToCEM_ SLOT9D2
91	ToCEM_ SLOT6D3	ToCEM_ SLOT6CK	LGND	ToCEM_ SLOTCK1	ToCEM_ SLOT9D3
92	FrCEM_ SLOT6D2	FrCEM_ SLOT6D1	BKPLN_ID0	FrCEM_ SLOT9D1	FrCEM_ SLOT9D2
93	FrCEM_ SLOT6D3	FrCEM_ SLOT6CK	LGND	FrCEM_ SLOT9CK1	FrCEM_ SLOT9D3
94	LGND	RED_LEDCTL_ A	LGND	RED_LEDCTL_ B	PCIU_FAIL
95	GREEN_LEDC TL_A	SHLFL_A	CUFAIL	SHLFL_B	GREEN_LEDC TL_B

NTLX82AA CEM (continued)

(Sheet 7 of 7)

96	FRAMELEDTST	PRES_OPER_A	MCTL	PRES_OPER_B	LGND
97	MEN	MPR	LGND	MCLK	SPR1
98	MMD	LGND	LGND	LGND	MSD

The following table shows the NTLX82AA CEM power pinning.

Pin	A	B	C	D	E
2	-48B	-48B	-48B	-48B	-48B
3	NC	NC	NC	NC	NC
4	NC	NC	NC	NC	NC
5	RTN	RTN	RTN	RTN	RTN
6	NC	NC	NC	NC	NC
7	NC	NC	NC	NC	NC
8	-48A	-48A	-48A	-48A	-48A

Technical data

This section describes the power and memory requirements for the NTLX82AA CEM.

Power requirements

The NTLX82AA CEM uses Lucent PUPS.

The following table shows the NTLX82AA CEM general power requirements.

(Sheet 1 of 2)

Parameter	Minimum	Nominal	Maximum	Units	Comments
Supply voltage	4.75	5.00	5.25	V	
Supply voltage				V	
Supply ripple				mV	

NTLX82AA CEM (end)

(Sheet 2 of 2)

Parameter	Minimum	Nominal	Maximum	Units	Comments
Supply current					
Power					Maximum allowed for 56 mm module

Memory

The NTLX82AA CEM uses 128 megabytes of memory, and it uses 96 megabytes of FLASH memory.

NTLX82BA CEM

Product description

The NTLX82BA common equipment module (CEM) provides the centralized resources required to support DMS-Spectrum Peripheral Module (SPM) applications. The NTLX82BA CEM is a replacement for NTLX82AA CEM.

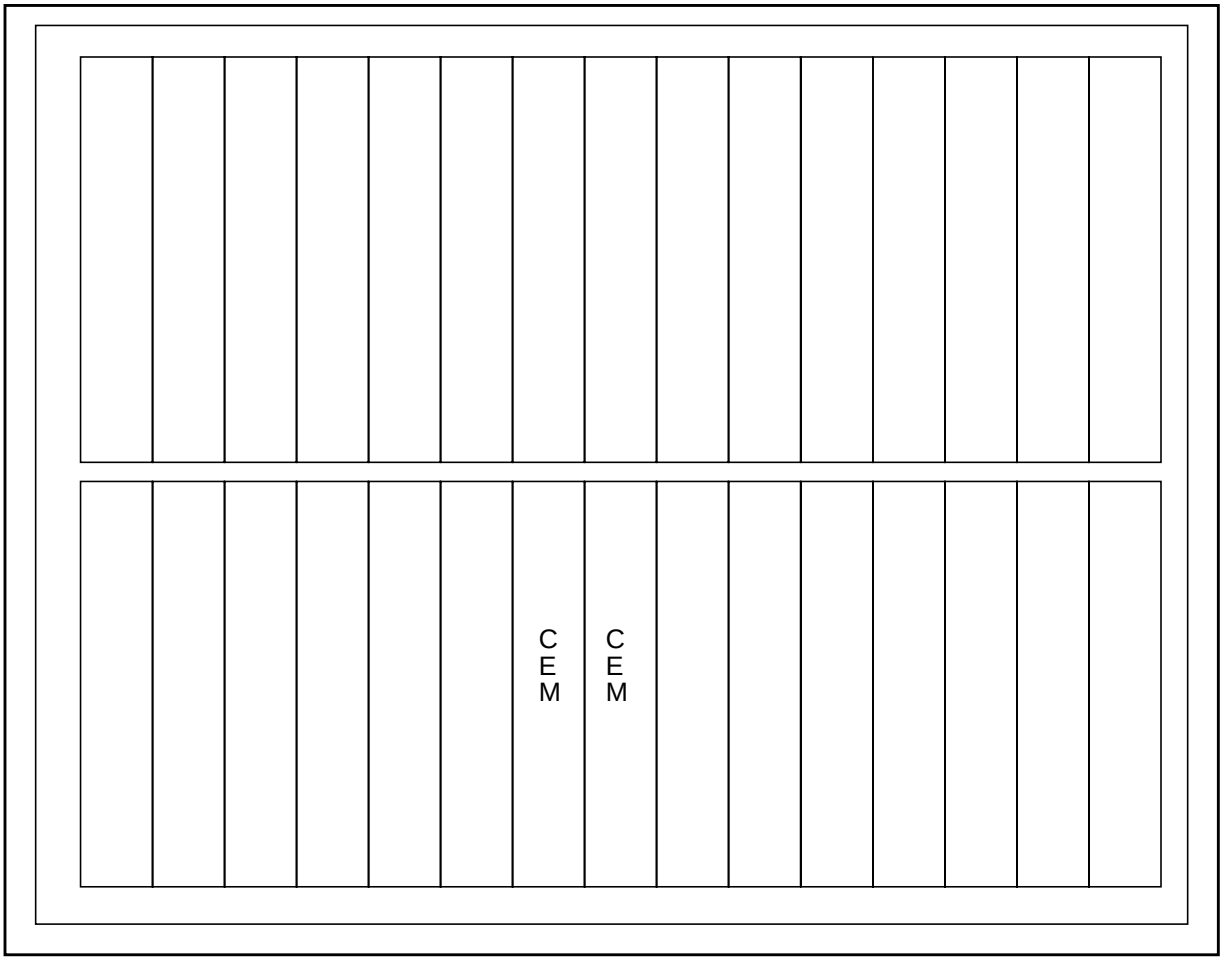
The following are the enhancements available when NTLX82AA CEM is upgraded to the NTLX82BA CEM:

- The new CEM (NTLX82BA) uses a PPC 750 processor chip, which replaces the PPC 603e.
- The internal instruction clock speed has increased from 100 MHz to 350 MHz.
- The L2 cache has been increased from 512 KB of 66 MHz SRAM to 1 MB of 140 MHz SRAM.
- The new CEM uses an AMD 79975 Ethernet chip, which replaces the AMD 79970.
- The SYNCP chip has been upgraded from the 68307 to the 68360, which provides 1 MB SRAM.
- The compute platform has been upgraded from 128 MB of 66 MHz EDO RAM to 128 MB of 100 MHz SDRAM.

Location

The two NTLX82BA CEMs are located in slots 7 and 8 on shelf 0 of the NTLX51AA or BA dual-shelf assembly.

SPM Shelf with two CEM cards



Functional description

The NTLX82BA CEM pair provides the following functions:

- bandwidth allocation
- communication and messaging
- computing platform
- network synchronization and timing subsystem
- 1 + 1 redundancy

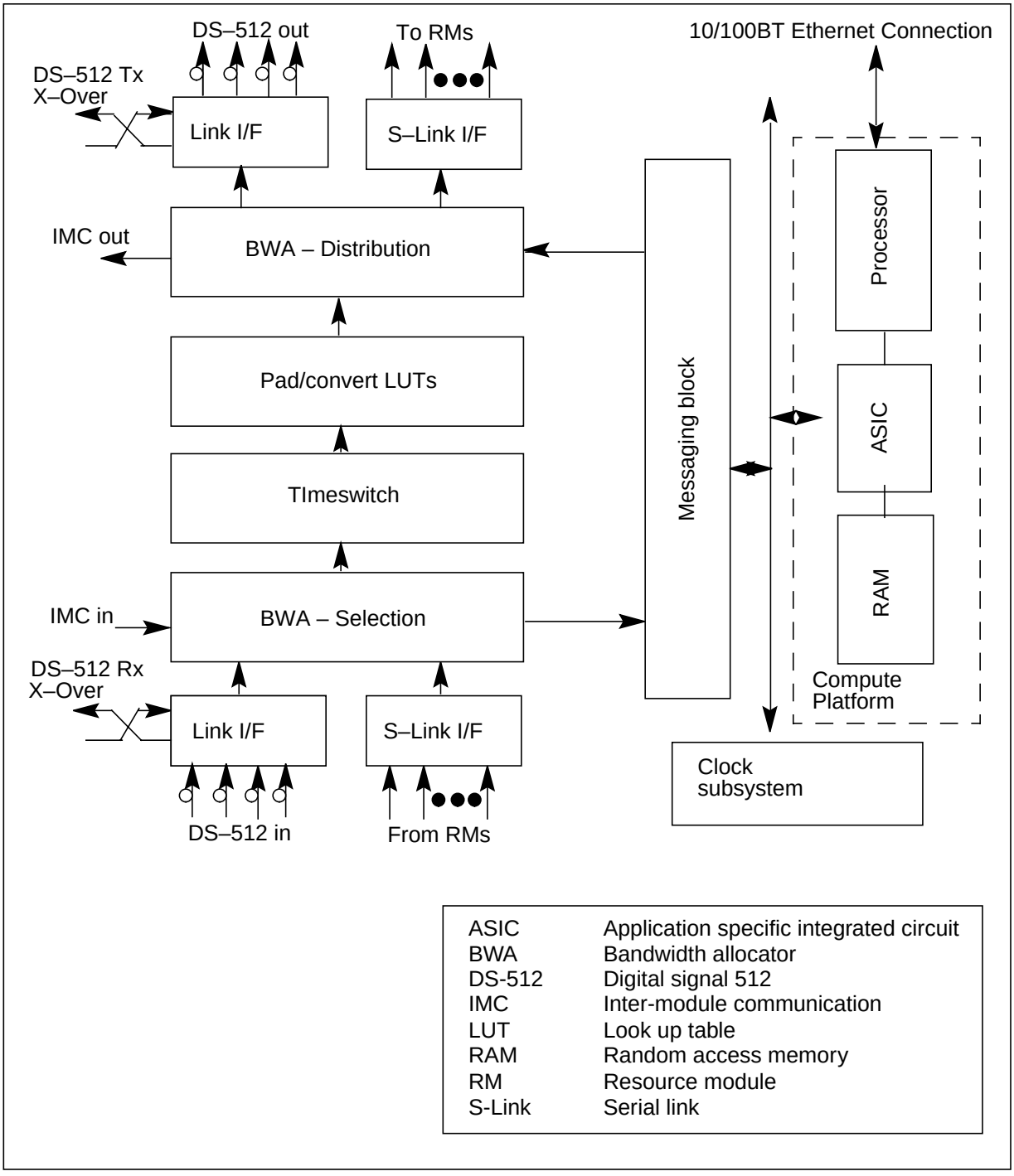
NTLX82BA CEM (continued)

Functional blocks

NTLX82BA CEM has the following functional blocks:

- DS-512 link interface
- S-Link interface
- bandwidth allocator
- timeswitch
- pad/convert LUTs
- messaging block
- compute platform
- clock subsystem

NTLX82BA CEM functional blocks



ASIC	Application specific integrated circuit
BWA	Bandwidth allocator
DS-512	Digital signal 512
IMC	Inter-module communication
LUT	Look up table
RAM	Random access memory
RM	Resource module
S-Link	Serial link

NTLX82BA CEM (continued)

DS-512 Link Interface

The DS-512 interface is shown in two parts, receive and transmit. When receiving, this block is responsible for:

- recovering the data and frame from the DS-512 link, including O/E and 12B10B conversion
- monitoring link status
- performing slip buffering, to enable the operation in the presence of a synchronization fault between the SPM and the network
- performing crossover of received data with the other CEM by means of the Rx crossover bus
- accommodating (small) phase differences between the two CEMs using elastic stores
- extracting the message channel (separate from PCM to reduce delay, and thus improve messaging performance)
- extracting and detecting the channel supervisory message (CSM) on both planes
- selecting the plane of PCM channels between the enhanced network (ENET) planes, on a per DS-0 basis

When transmitting, this block is responsible for:

- combining host messaging timeslots with those of the mate CEM (when required)
- inserting CSM data
- accepting PCM timeslots from the active CEM by means of the Tx crossover bus, when this CEM is inactive
- performing the 10B12B conversion, inserting the framing channel and performing E/O conversion
- generating the link transmit clock, phase locked to the active CEM system clock (this enables operation of these links, even if the system clock on this CEM is inoperative

Physically, this block is implemented with the following two ASICs:

- quad link controller (QLC)
- CSM & plane select device

S-Link Interface

The S-Link interface is shown in two parts: receive and transmit. This block is responsible for converting the parallel data format used on the CEM and the

256 timeslot serial links to interface with the resource modules. In addition, it distributes the system clock to the resource modules, and provides low level control and status by means of overhead bits embedded in the S-Link format.

Physically, this block is composed of 6 identical S-Link interface master devices (SLIF-M), each processing 16 S-Links.

Bandwidth Allocator

The bandwidth allocator (BWA) function is shown in two parts, selection (BWA-S) and distribution (BSWA-D). This block operates much like a double buffered timeswitch, except it cycles over 32 times per frame. Thus, it has a connection resolution of 128 timeslots, and an average through delay (each side) of 1/32 frame. Each set of 32 timeslots is referred to as a bandwidth allocator group. Each component (BWA-S and BWA-D) is capable of broadcast connections.

The BWA is an asymmetrical matrix, with 26K timeslots (768 P-side & 64 C-side BWA groups) on the S-Link side, and 12K timeslots (384 BWA groups) on the timeswitch side.

This block is used to:

- groom platform overhead timeslots from the S-Links to the timeswitch, and vice-versa, allowing for variations in timeslot usage by various RMs
- merge selectively the C-side timeslot stream with those from the S-Links
- apply digital padding (selectable on a per-DS-0 basis) to timeslots from the timeswitch
- extract and insert messaging channels from the timeslot stream, and present them to the messaging block
- assist in RM sparing, by providing a mechanism by which traffic can be rapidly switched between RMs

Timeswitch

The timeswitch provides single timeslot rearrangement functions. It has 12K timeslots, and is a double buffered (N x DS-0 capable) design, based on ENET components. The timeswitch receives input from the BWA and acts as a matrix. Together with the BWA, it maps the C-side DS-512 channels to P-side channels on the SPM backplane. Those P-side channels connect to RMs. Therefore the timeswitch is a key component in mapping DS-0 connections from the ENET to the RMs that transport signals like the OC3 or ATM RM.

NTLX82BA CEM (continued)

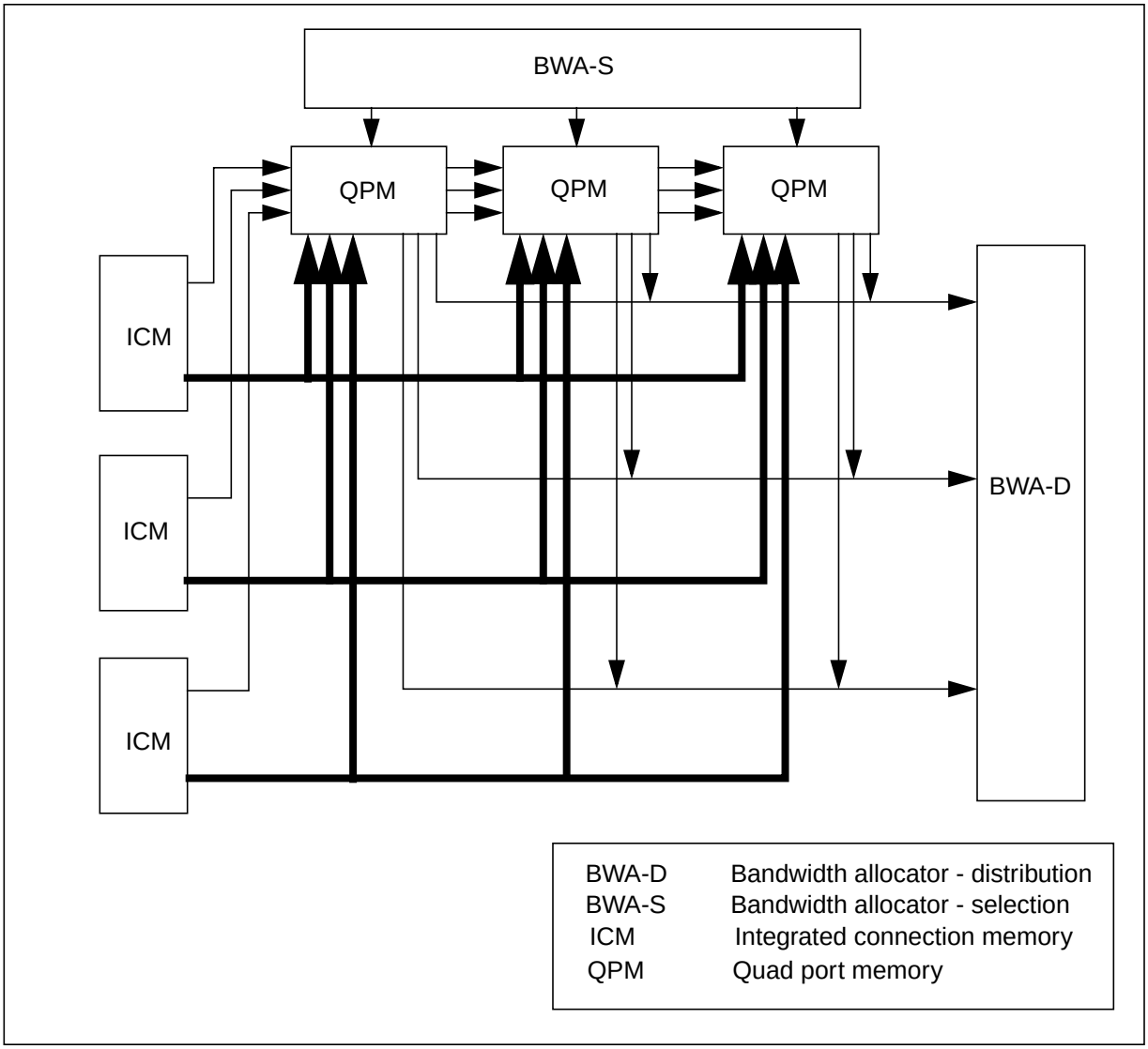
Physically, it is composed of six devices:

- three quad port memory (QPM) ASICs
- three integrated connection memory (ICM) ASICs

The following figure illustrates how the timeswitch does the following.

- receives input from the bandwidth allocator - selection (BWA-S)
- integrated connection memory (ICM) maps the input and output ports on the quad port memory (QPM) to the bandwidth allocator - distribution (BWA-D)
- QPM chips transfer data from BWA-S to the BWA-D

Timeswitch functional illustration



Pad/convert LUTs

The padding look up tables (LUTs) module provides a generalized PCM conversion facility, normally used to implement gain and loss padding as required for the gain/loss plan. It provides up to 16 conversion tables, selectable on a per-DS-0 basis for the 12K timeslot stream from the timeswitch. Table selection is provided by means of bits from the ICM ASICs used to control the timeswitch. It is implemented as a function of the BWA ASIC in distribution mode.

NTLX82BA CEM (continued)

Messaging block

This block provides DMS protocol messaging functionality. Up to 32 messaging ports can be provisioned. Each port is capable of N x DS-0 bandwidth. Each port can be provisioned to use one of the following protocols:

- DMS-Y for messaging to the message switch (MS) and core
- DMS-W for messaging internal to the SPM

The messaging ports are used for host messaging (4 ports), RM messaging (26 ports), IMC messaging (1 port), and 1 spare port for diagnostics.

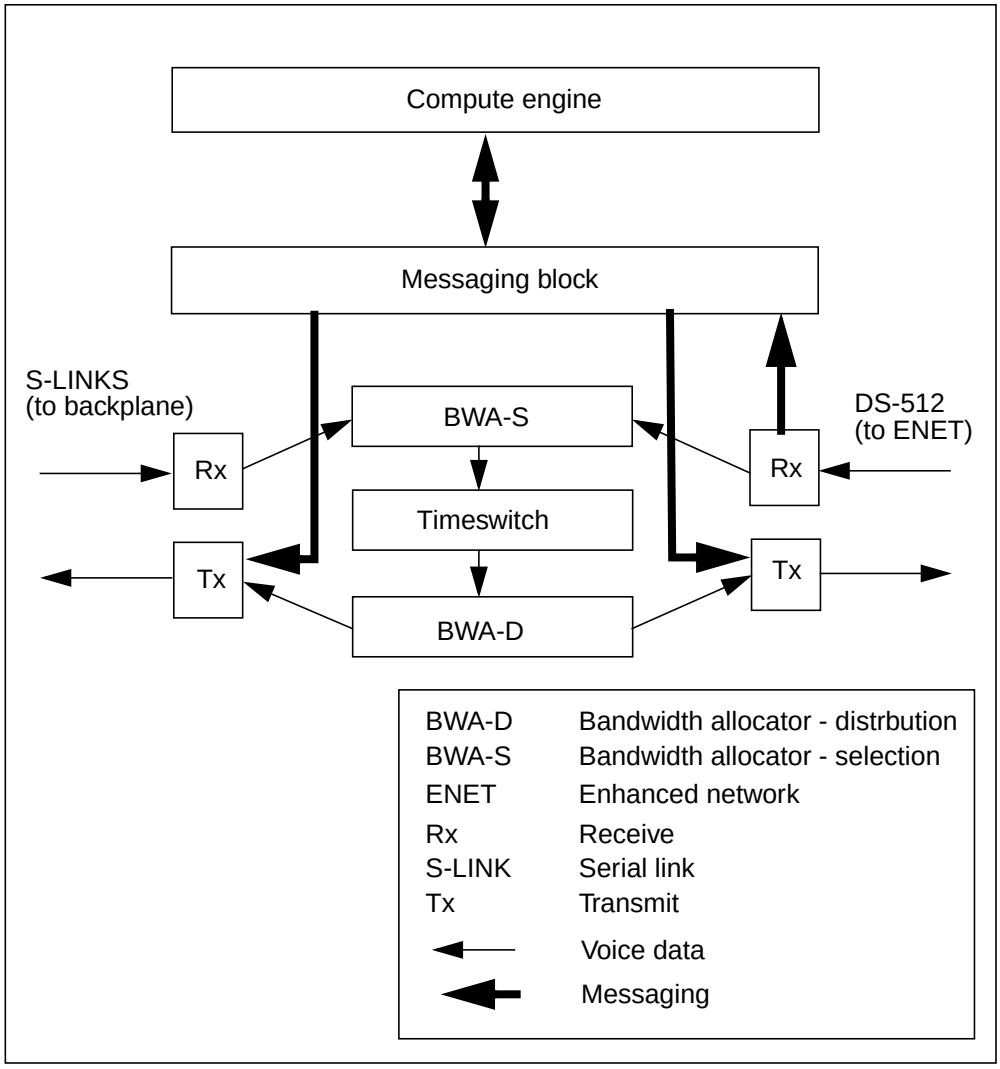
This block can terminate messages by DMA access into the processor memory.

Physically it is composed of

- one link protocol messaging interface controller (LPMIC) ASIC
- one integrated connection memory (ICM)

The following figure indicates how the messaging block relates to the compute engine, the DS-512 transmit and receive interfaces, and the bandwidth allocator blocks. Through the bandwidth allocator - distribution (BWA-D), the messaging block communicates with the resource modules (RM) in the SPM.

Messaging block functional diagram



Compute Platform

The CEM main processor is implemented with a multi-chip module (MCM) processor block. It has 128 MB of 100MHz DRAM and 96 MB Flash as well as 100/10BT Ethernet connection

Clock Subsystem

This clock is responsible for generating the SPM system clock. It can generate a clock phase locked (8 KHz) to either plane of the network by means of a DS-512 link, or phase information acquired from a RM slot. It is implemented with a small microprocessor (68360), digital to analog converter, and the TIC ASIC. This block also determines common equipment module activity and

NTLX82BA CEM (continued)

coordinates SWitch of ACTivity (SWACT). The clock from this subsystem is distributed to the RMs by means of the S-Links.

Miscellaneous

In addition to the above, the CEM contains support for test functions (JTAG) provided by an integrated testbus master (ITM) ASIC, and alarm and visual indicator LED control.

Signaling

The following table shows NTLX82BA CEM backplane connections.

(Sheet 1 of 7)

Pin	A	B	C	D	E
2	LGND	LGND	LGND	LGND	LGND
3	ToCEM_ SLOT22D2	ToCEM_ SLOT22D1	LGND	ToCEM_ SLOT23D2	ToCEM_ SLOT23D2
4	ToCEM_ SLOT22D3	ToCEM_ SLOT22CK	LGND	ToCEM_ SLOT23CK	ToCEM_ SLOT23D3
5	FrCEM_ SLOT22D2	FrCEM_ SLOT22D1	LGND	FrCEM_ SLOT23D1	FrCEM_ SLOT23D2
6	FrCEM_ SLOT22D3	FrCEM_ SLOT22CK	LGND	FrCEM_ SLOT23CK	FrCEM_ SLOT23D3
7	ToCEM_ SLOT21D2	ToCEM_ SLOT21D1	LGND	ToCEM_ SLOT24D1	ToCEM_ SLOT24D2
8	ToCEM_ SLOT21D3	ToCEM_ SLOT21CK	LGND	ToCEM_ SLOT24CK	ToCEM_ SLOT24D3
9	FrCEM_ SLOT21D2	FrCEM_ SLOT21D1	LGND	FrCEM_ SLOT24D1	FrCEM_ SLOT24D2
10	FrCEM_ SLOT21D3	FrCEM_ SLOT21CK	LGND	FrCEM_ SLOT24CK	FrCEM_ SLOT24D3
11	LGND	LGND	LGND	ToCEM_ SLOT25D1	ToCEM_ SLOT25D2
12	ToCEM_ SLOT20D2	ToCEM_ SLOT20D1	LGND	ToCEM_ SLOT25CK	ToCEM_ SLOT25D3

(Sheet 2 of 7)

13	ToCEM_ SLOT20D3	ToCEM_ SLOT20CK	LGND	FrCEM_ SLOT25D1	FrCEM_ SLOT25d2
14	FrCEM_ SLOT20D2	FrCEM_ SLOT20D1	LGND	FrCEM_ SLOT25CK	FrCEM_ SLOT25D3
15	FrCEM_ SLOT20D3	FrCEM_ SLOT20CK	LGND	LGND	LGND
16	ToCEM_ SLOT19D2	ToCEM_ SLOT19D1	LGND	ToCEM_ SLOT26D1	ToCEM_ SLOT26D2
17	ToCEM_ SLOT19D3	ToCEM_ SLOT19CK	LGND	ToCEM_ SLOT26CK	ToCEM_ SLOT26D3
18	ToCEM_ SLOT19D2	FrCEM_ SLOT19D1	LGND	FrCEM_ SLOT26D1	FrCEM_ SLOT26D2
19	FrCEM_ SLOT19D3	FrCEM_ SLOT19CK	LGND	FrCEM_ SLOT26CK	FrCEM_ SLOT26D3
20	ToCEM_ Sp17D	ToCEM_ Sp17CK	LGND	ToCEM_ SLOT27D1	ToCEM_ SLOT27D2
21	FrCEM_ Sp17D	FrCEM_ Sp17CK	LGND	ToCEM_ SLOT27CK	ToCEM_ SLOT27D3
22	LGND	LGND	LGND	FrCEM_ SLOT27D1	FrCEM_ SLOT27D2
23	ToCEM_ SLOT18D2	ToCEM_ SLOT18D1	LGND	FrCEM_ SLOT27CK	FrCEM_ SLOT27D3
24	ToCEM_ SLOT18D3	ToCEM_ SLOT18D2	LGND	ToCEM_ SLOT28D1	ToCEM_ SLOT28D2
25	FrCEM_ SLOT18D2	FrCEM_ SLOT18D1	LGND	ToCEM_ SLOT28CK	ToCEM_ SLOT28D3
26	FrCEM_ SLOT18D3	FrCEM_ SLOT18CK	LGND	FrCEM_ SLOT28D1	FrCEM_ SLOT28D2
27	ToCEM_ SLOT17D2	ToCEM_ SLOT17D1	LGND	FrCEM_ SLOT28CK	FrCEM_ SLOT28D3
28	ToCEM_ SLOT17D3	ToCEM_ SLOT17CK	LGND	LGND	LGND

NTLX82BA CEM (continued)

(Sheet 3 of 7)

29	FrCEM_ SLOT17D2	FrCEM_ SLOT17D1	LGND	ToCEM_ SLOT14D1	ToCEM_ SLOT14D2
30	FrCEM_ SLOT17D3	FrCEM_ SLOT17CK	LGND	ToCEM_ SLOT14CK	ToCEM_ SLOT14D3
31	ToCEM_ SLOT16D2	ToCEM_ SLOT16D1	LGND	FrCEM_ SLOT14D1	FrCEM_ SLOT14D3
32	ToCEM_ SLOT16D3	ToCEM_ SLOT16CK	LGND	FrCEM_ SLOT14CK	FrCEM_ SLOT14D3
33	FrCEM_ SLOT16D2	FrCEM_ SLOT16D1	LGND	ToCEM_ SLOT13D1	ToCEM_ SLOT13D2
34	FrCEM_ SLOT16D3	FrCEM_ SLOT16CK	LGND	ToCEM_ SLOT13CK	ToCEM_ SLOT13D3
35	ToCEM_ Sp15D	ToCEM_ Sp15CK	LGND	FrCEM_ SLOT13D1	FrCEM_ SLOT13D2
36	FrCEM_ Sp15D	FrCEM_ Sp15CK	LGND	FrCEM_ SLOT13CK	FrCEM_ SLOT13D3
37	ToMATE_ QLC	FrMATE_ QLC	LGND	LGND	LGND
38	ToMATE_ RXPCM0	ToMATE_ RXPCM1	LGND	FrMATE_ RXPCM1	FrMATE_ RXPCM0
39					
40	ToMATE_ RXPCM2	ToMATE_ RXPCM3	LGND	FrMATE_ RXPCM3	FrMATE_ RXPCM2
41	ToMATE_ RXPCM4	ToMATE_ RXPCM5	LGND	FrMATE_ RXPCM5	FrMATE_ RXPCM4
42	ToMATE_ RXPCM6	ToMATE_ RXPCM7	ToMATE_ RXPCM8	FrMATE_ RXPCM7	FrMATE_ RXPCM6
43	ToMATE_ RXPCM_FPN	ToMATE_ RXPCM9	FrMATE_ RXPCM8	FrMATE_ RXPCM9	FrMATE_ RXPCM_FPN
44	ToMATE_ CSIDE	ToMATE_ RXPCM_CLK	LGND	FrMATE_ RXPCM_CLK	FrMATE_ CSIDE
45	ToMATE_ TXPCM0	ToMATE_ DS1	LGND	FrMATE_ DS1	FrMATE_ TXPCM0

(Sheet 4 of 7)

46	ToMATE_ TXPCM2	ToMATE_ TXPCM1	LGND	FrMATE_ TXPCM1	FrMATE_ TXPCM2
47	ToMATE_ TXPCM4	ToMATE_ TXPCM3	LGND	FrMATE_ TXPCM3	FrMATE_ TXPCM4
48	ToMATE_ TXPCM7	ToMATE_ TXPCM5	ToMATE_ TXPCM6	FrMATE_ TXPCM5	FrMATE_ TXPCM7
49	ToMATE_ TXPCM9	ToMATE_ TXPCM8	FrMATE_ TXPCM6	FrMATE_ TXPCM8	FrMATE_ TXPCM9
50	ToMATE_ TXPCM_FPN	ToMATE_ TXPCM10	LGND	FrMATE_ TXPCM10	FrMATE_ TXPCM_FPN
51	ToMATE_ IMC0	ToMATE_ TXPCM_CLK	LGND	FrMATE_ TXPCM_CLK	FrMATE_ IMC0
52	ToMATE_ IMC2	ToMATE_ IMC1	LGND	FrMATE_ IMC1	FrMATE_ IMC2
53	ToMATE_ IMC4	ToMATE_ IMC3	LGND	FrMATE_ IMC3	FrMATE_ IMC4
54	ToMATE_ IMC_FPN	ToMATE_ IMC_CLK	ToMATE_ ACT	FrMATE_ IMC_CLK	FrMATE_ IMC_FPN
55	ToMATE_ SFPN	ToMATE_ PRES	FrMATE_ ACT	FrMATE_ PRES	FrMATE_ SFPN
56	ToMATE_ RSTREQ	ToMATE_ TOD	ToMATE_ ACTDROP	FrMATE_ TOD	FrMATE_ RSTREQ
57	ToMATE_ SYS_FPN	ToMATE_ SYS_CLK	FrMATE_ ACTDROP	FrMATE_ SYS_CLK	FrMATE_ SYS_FPN
58	LGND	LGND	ToMATE_ FAIL	LGND	LGND
59	ToCEM_ SLOT15D2	ToCEM_ SLOT15D1	FrMATE_ FAIL	ToCEM_ SLOT12D1	ToCEM_ SLOT12D2
60	ToCEM_ SLOT15D3	ToCEM_ SLOT15CK	LGND	ToCEM_ SLOT12CK	ToCEM_ SLOT12D3
61			LGND		
62	FrCEM_ SLOT15D2	FrCEM_ SLOT15D1	LGND	FrCEM_ SLOT12D1	FrCEM_ SLOT12D2
63	FrCEM_ SLOT15D3	FrCEM_ SLOT15CK	LGND	FrCEM_ SLOT12CK	FrCEM_ SLOT12D3

NTLX82BA CEM (continued)

(Sheet 5 of 7)

64	ToCEM_ Sp1D	ToCEM_ Sp1CK	LGND	ToCEM_ SLOT11D1	ToCEM_ SLOT11D2
65	FrCEM_ Sp1D	FrCEM_ Sp1CK	LGND	FrCEM_ SLOT11CK	FrCEM_ SLOT11D3
66	ToCEM_ SLOT1D2	ToCEM_ SLOT1D1	LGND	FrCEM_ SLOT11D1	FrCEM_ SLOT11D2
67	ToCEM_ SLOT1D3	ToCEM_ SLOT1CK	LGND	FrCEM_ SLOT11CK	FrCEM_ SLOT11D3
68	FrCEM_ SLOT1D2	FrCEM_ SLOT1D1	LGND	LGND	LGND
69	FrCEM_ SLOT1D3	FrCEM_ SLOT1CK	SYNC_FrSRMO	ToCEM_ SLOT10D7	ToCEM_ SLOT10D8
70	ToCEM_ SLOT2D2	ToCEM_ SLOT2D1	LGND	ToCEM_ SLOT10CK3	ToCEM_ SLOT10D9
71	ToCEM_ SLOT2D3	ToCEM_ SLOT2CK	LGND	FrCEM_ SLOT10D7	FrCEM_ SLOT10D8
72	FrCEM_ SLOT2D2	FrCEM_ SLOT2D1	LGND	FrCEM_ SLOT10CK3	FrCEM_ SLOT10D9
73	FrCEM_ SLOT2D3	FrCEM_ SLOT2CK	LGND	ToCEM_ SLOT10D4	FrCEM_ SLOT10D5
74	LGND	LGND	LGND	ToCEM_ SLOT10CK2	ToCEM_ SLOT10D6
75	ToCEM_ Sp3D	ToCEM_ Sp3CK	SYNC_FrOC3_ 1	FrCEM_ SLOT10D4	FrCEM_ SLOT10D5
76	FrCEM_ Sp3D	FrCEM_ Sp3CK	LGND	FrCEM_ SLOT10CK2	FrCEM_ SLOT10D6
77	ToCEM_ SLOT3D2	ToCEM_ SLOT3D1	LGND	ToCEM_ SLOT10D1	ToCEM_ SLOT10D2
78	ToCEM_ SLOT3D3	ToCEM_ SLOT3CK	SYNC_FrSRM_ 1	ToCEM_ SLOT10CK1	ToCEM_ SLOT10D3
79	FrCEM_ SLOT3D2	FrCEM_ SLOT3D1	LGND	FrCEM_ SLOT10D1	FrCEM_ SLOT10D2

(Sheet 6 of 7)

80	FrCEM_ SLOT3D3	FrCEM_ SLOT3CK	LGND	FrCEM_ SLOT10CK1	FrCEM_ SLOT10D3
81	ToCEM_ SLOT4D2	ToCEM_ SLOT4D1	LGND	LGND	LGND
82	ToCEM_ SLOT4D3	ToCEM_ SLOT4CK	CEM_SLOT_ID	ToCEM_ SLOT9D7	ToCEM_ SLOT9D8
83	FrCEM_ SLOT4D2	FrCEM_ SLOT4D1	LGND	ToCEM_ SLOT9CK3	ToCEM_ SLOT9D9
84	FrCEM_ SLOT4D3	FrCEM_ SLOT4CK	BKPLN_ID3	FrCEM_ SLOT9D7	FrCEM_ SLOT9D8
85	LGND	LGND	LGND	FrCEM_ SLOT9CK3	FrCEM_ SLOT9D8
86	ToCEM_ SLOT5D2	ToCEM_ SLOT5D1	SYNC_FrOC3_ 0	ToCEM_ SLOT9D4	ToCEM_ SLOT9D5
87	ToCEM_ SLOT5D3	ToCEM_ SLOT5CK	LGND	ToCEM_ SLOT9CK2	ToCEM_ SLOT9D6
88	FrCEM_ SLOT5D2	FrCEM_ SLOT5D1	BKPLN_ID2	FrCEM_ SLOT9D4	FrCEM_ SLOT9D5
89	FrCEM_ SLOT5D3	FrCEM_ SLOT5CK	LGND	FrCEM_ SLOT9CK2	FrCEM_ SLOT9D6
90	ToCEM_ SLOT6D2	ToCEM_ SLOT6D1	BKPLN_ID1	ToCEM_ SLOT9D1	ToCEM_ SLOT9D2
91	ToCEM_ SLOT6D3	ToCEM_ SLOT6CK	LGND	ToCEM_ SLOTCK1	ToCEM_ SLOT9D3
92	FrCEM_ SLOT6D2	FrCEM_ SLOT6D1	BKPLN_ID0	FrCEM_ SLOT9D1	FrCEM_ SLOT9D2
93	FrCEM_ SLOT6D3	FrCEM_ SLOT6CK	LGND	FrCEM_ SLOT9CK1	FrCEM_ SLOT9D3
94	LGND	RED_LEDCTL_ A	LGND	RED_LEDCTL_ B	PCIU_FAIL
95	GREEN_LEDC TL_A	SHLFL_A	CUFAIL	SHLFL_B	GREEN_LEDC TL_B

NTLX82BA CEM (continued)

(Sheet 7 of 7)

96	FRAMELEDTST	PRES_OPER_A	MCTL	PRES_OPER_B	LGND
97	MEN	MPR	LGND	MCLK	SPR1
98	MMD	LGND	LGND	LGND	MSD

The following table shows the NTLX82BA CEM power pinning.

Pin	A	B	C	D	E
2	-48B	-48B	-48B	-48B	-48B
3	NC	NC	NC	NC	NC
4	NC	NC	NC	NC	NC
5	RTN	RTN	RTN	RTN	RTN
6	NC	NC	NC	NC	NC
7	NC	NC	NC	NC	NC
8	-48A	-48A	-48A	-48A	-48A

Technical data

This section describes the power and memory requirements for the NTLX82BA CEM.

Power requirements

The NTLX82BA CEM uses Lucent PUPS.

The following table shows the NTLX82BA CEM general power requirements.

(Sheet 1 of 2)

Parameter	Minimum	Nominal	Maximum	Units	Comments
Supply voltage	4.75	5.00	5.25	V	
Supply voltage				V	
Supply ripple				mV	

(Sheet 2 of 2)

Parameter	Minimum	Nominal	Maximum	Units	Comments
Supply current					
Power					Maximum allowed for 56 mm module

Memory

The NTLX82BA CEM uses 128 megabytes of memory, and it uses 96 megabytes of FLASH memory.

NTLX85/86AA VSP RM

Description

The NTLX85/86AA voice signal processor (VSP) resource module (RM) provides resources for call processing such as echo cancellation for the DMS-Spectrum Peripheral Module (SPM).

Note: The NTLX85/86AA VSP RM is an OEM product that is sometimes referred to as an echo canceller resource module, or ECRM.

Location

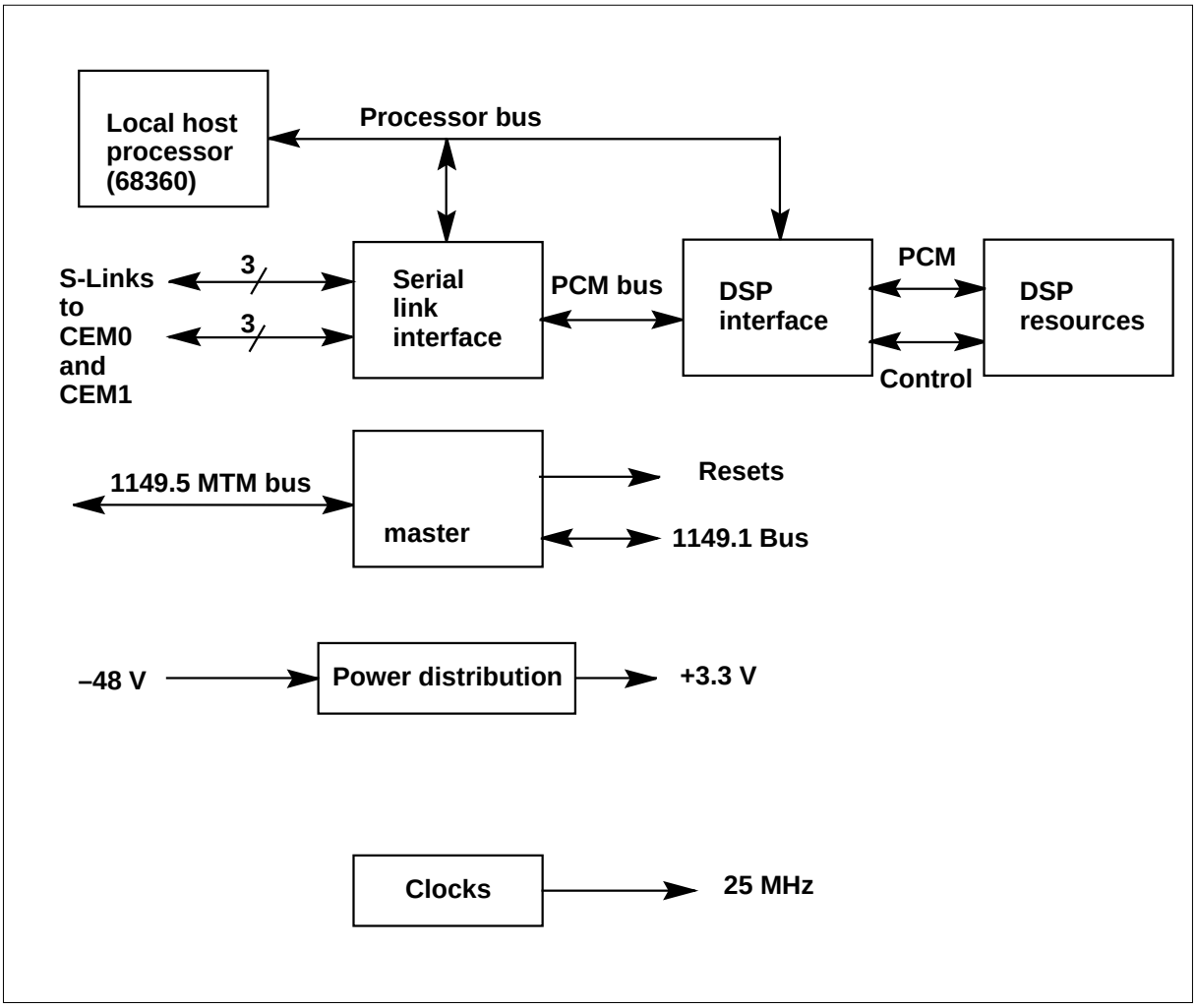
The NTLX85/86AA VSP RM optionally occupies slots 3 through 4 and 13 through 14 on shelf 0, and slots 5 through 6 and 14 on shelf 1 of the NTLX51BA dual-shelf assembly. The quantities and locations of VSP RM are office dependent.

Functional blocks

The NTLX85/86AA VSP RM has the following functional blocks:

- computing platform
- serial link interface
- intelligent test bus master (ITM)
- clocks
- power distribution
- DSP interface
- DSP resources

The following figure shows the functional block diagram of the VSP RM.



Computing platform

The computing platform is the NTLX85/86AA VSP RM central processing complex. It contains built-in serial communication controllers, dynamic random access memory, timers, debug port, and direct memory access controllers. Software loads are contained in flash-erasable programmable read-only memory (EPROM), which load directly to random access memory (RAM).

Serial link interface

The serial link interface provides messaging and pulse code modulation interfaces between the two common equipment modules (CEM) and the host processor.

NTLX85/86AA VSP RM (continued)

ITM

The ITM consists primarily of power-ip reset and boundary-scan logic, and includes an interface to the MIM.

Clock

The clock provides a 25 MHz clock. The 25 MHz clock is used by the host processor, the serial link interface, and the DSP resources.

Power distribution

The power distribution function uses a -48 to +3 volt dc-to-dc converter and its associated filters to provide power to the other functions.

DSP interface

The DSP interface block provides the following services:

- address decoding
- interrupt generation
- control interface to DSP resources
- PCM formatting

DSP resources

The DSP resources perform the following primary functions:

- echo cancellation
- performance monitoring

Signaling

The following table lists the NTLX85/86AA VSP RM backplane pin description.

(Sheet 1 of 2)

Signal	Function	IO Type	Description
-48A	power	-	-48 V battery feed A
-48B	power	-	-48 V battery feed B
RTN	power	-	Battery return
FrCEMnCK	input	3.3V CMOS SLIF-S	S-link clock lines from common equipment (n = 0 CEM0, n = 1 CEM1)
FrCEMnDm	input	3.3V CMOS SLIF-S	S-link clock lines from common equipment (n = 0 CEM0, n = 1 CEM1, m = 1, 2, 3)

(Sheet 2 of 2)

Signal	Function	IO Type	Description
ToCEMnCK	output	3.3V CMOS SLIF-S	S-link clock lines from common equipment (n = 0 CEM0, n = 1 CEM1)
ToCEMnDM	output	3.3V CMOS SLIF-S	S-link clock lines from common equipment (n = 0 CEM0, n = 1 CEM1, m = 1, 2, 3)
MMD	input	3.3V CMOS ITM	JTAG 1149.5 bus master data
MSD	input/output open drain	3.3V CMOS ITM	JTAG 1149.5 bus slave data
MCLK	input	3.3V CMOS ITM	JTAG 1149.5 bus clock
MPR	input output open drain	3.3V CMOS ITM	JTAG 1149.5 bus request
MCT	input	3.3V CMOS ITM	JTAG 1149.5 bus control
SLOT_IDn	input	GND/NC	RM slot ID (n = 0, 1, 2, 3, 4) (pin is either grounded on backplane or floating)
LGND	power	-	Logic ground of the PCP/BACKPLANE

The following table lists the NTLX85/86AA VSP RM backplane 1SU power connector pin description.

Pin	A	B	C	D	E
2	-48B	-48B	-48B	-48B	-48B
3	NC	NC	NC	NC	NC
4	NC	NC	NC	NC	NC
5	RTN	RTN	RTN	RTN	RTN
6	NC	NC	NC	NC	NC
7	NC	NC	NC	NC	NC
8	-48A	-48A	-48A	-48A	-48A

NTLX85/86AA VSP RM (continued)

The following table lists the NTLX85/86AA VSP RM backplane 2SU power connector pin description.

Pin	A	B	C	D	E
2	SYNC_toCEM0	LGND	LGND	LGND	SYNC_FrOC30
3	SYNC_toCEM1	ToSRM_Mate	LGND	FrSRM_Mate	SYNC_FrOC31
4	LGND	LGND	LGND	LGND	LGND
5	ToCEM0_SpD	ToCEM0_SpCK	LGND	ToCEM1_SpCK	ToCEM1_SpD
6	FrCEM0_SpD	FrCEM0_SpCK	LGND	FrCEM1_SpCK	FrCEM1_SpD
7	ToCEM0_D2	ToCEM0_D1	LGND	ToCEM1_D1	ToCEM1_D2
8	ToCEM0_D3	ToCEM0_CK	LGND	ToCEM1_CK	ToCEM1_D3
9	FrCEM0_D2	FrCEM0_D1	LGND	FrCEM1_D1	FrCEM1_D2
10	FrCEM0_D3	FrCEM0_CK	LGND	FrCEM1_CK	FrCEM1_D3
11	LGND	LGND	LGND	LGND	LGND
12	See Note 4.	See Note 4.	LGND	See Note 4.	See Note 4.
13	See Note 4.	See Note 4.	LGND	See Note 4.	See Note 4.
14	See Note 4.	See Note 4.	LGND	See Note 4.	See Note 4.
15	See Note 4.	See Note 4.	LGND	See Note 4.	See Note 4.
16	SLOT_ID4	SLOT_ID3	MTCL	SLOT_ID1	SLOT_ID0
17	LGND	MPR	SLOT_ID2	MCLK	LGND
18	MMD	LGND	LGND	LGND	MSD

Note 1: Pins 2B, 2C, 2D, 18B, 18C, and 18D are advanced pins.

Note 2: Connections for signals at pins 2A, 2E, 3A, 3B, and 3D are only made in slots 5 through 10. These are special signals distributed between the CEMs and the OC3 RMs. These pins are left as no-connects in all other slots. These signals are not used by the VSP.

Note 3: Spare S-links are terminated on pins 5ABDE and 6ABDE only in slots 1, 3, 15, and 17. These pins are left as no-connects in all other slots. These signlals are not used by the VSP.

Note 4: Pins 12-15 ABDE are reserved for future use. These pins may be used to fold over the S-link connections from the adjacent RM to provide increased bandwidth at a single RM slot. These signals are not used by the VSP.

The following table lists the BDM 10-pin (2 x 5) header pin description.

Pin	Signal	Signal	Pin number
1	DS	BERR	2
3	GND	BKPT/DSCLK	4
5	GND	FREEZE	6
7	RESETH	IFETCH/DSI	8
9	VDD	IPIP0/DSO	10

The following table lists the RS-232 connector pin description.

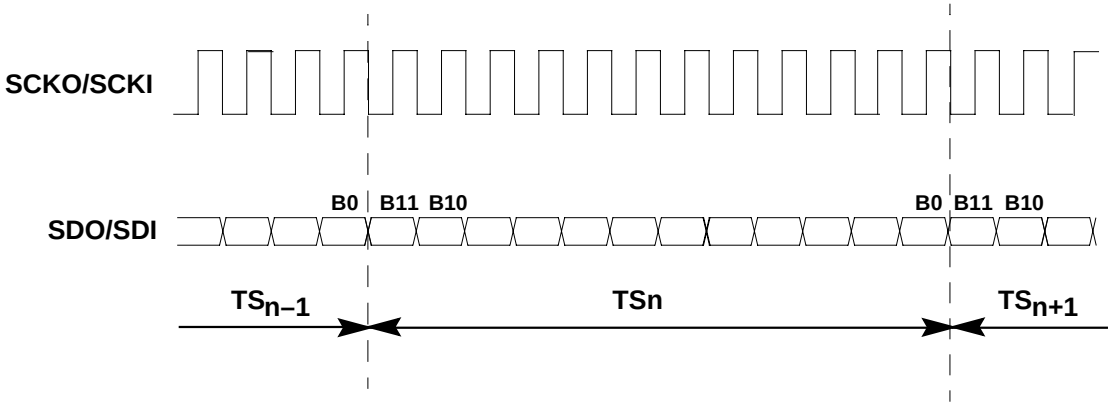
Pin	Signal	Signal	Pin number
1	not used	RX	2
3	TX	not used	4
5	GND	not used	6
7	RTS/TX2	IFETCH/CTS/RX2	8
9	not used		

Timing

Serial link interface timing

The following figure shows serial link interface timing.

NTLX85/86AA VSP RM (continued)

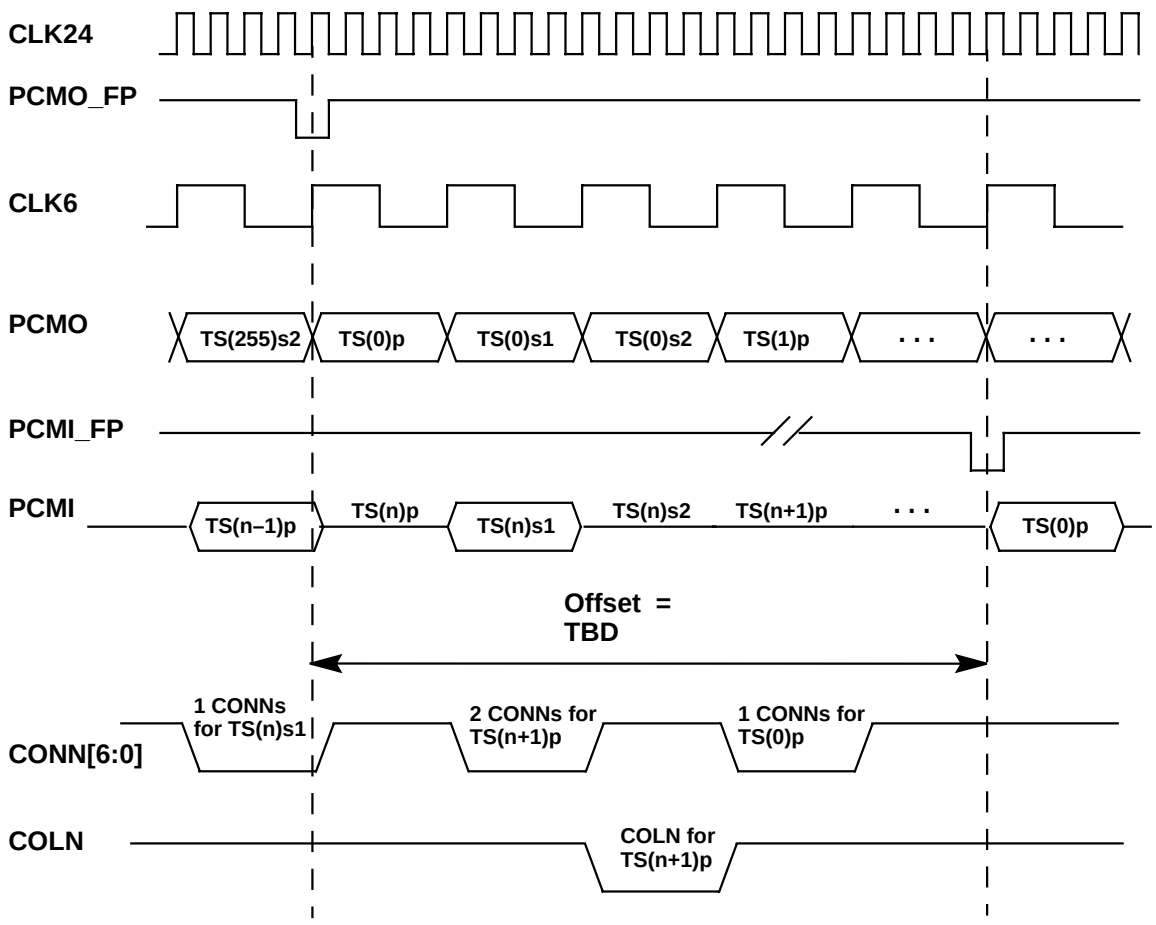


Legend:

SCKO	Serial clock out
SCKI	Serial clock in
SDO	Serial data in
SDI	Serial data out
B0, B1, B#	Bit of the serial data (each timeslot has 12 bits of data; that is Bit 0 through Bit 11)
TS	Timeslot

PCM bus timing

The following figure shows PCM bus timing.



Legend:

CLK24	24.756 MHz clock
PCMO_FP	PCM out frame pulse
CLK6	6.144 MHz clock
PCMO	PCM out (transmit)
PCMI_FP	PCM in frame pulse
PCMI	PCM in (receive)
Offset	offset between transmit and recieve PCM frames
CONN[6:0]	connection signals 0 through 6)
COLN	collision signal

NTLX85/86AA VSP RM (end)

Power requirements

The maximum power dissipation of the NTLX85/86AA VSP RM does not exceed 40 watts. The following table shows general power requirements.

Parameter	Minimum	Nominal	Maximum	Units	Condition
Supply voltage	3.10	3.30	03.50	V	
Supply noise			20.00	mV	
Supply current		5.0	6.0	A	

NTLX91BA SPM-DMS frame assembly

Description

In the North American market, DMS-Spectrum Peripheral Module (SPM) equipment installs in a standard DMS NTLX91BA frame assembly. The DMS NTLX91BA frame is normally provisioned to accommodate two SPM nodes, although it can be used in a single node configuration. The module allows for expansion by adding circuit packs, cabling, and power.

The NTLX91BA frame assembly is a replacement for the NTLX50AA frame assembly.

The NTLX91BA frame assembly consists of the following features:

- standard DMS racks
- adapter brackets for dual-shelf assemblies
- cable segregation for power, fiber, signaling, and alarms
- accommodation of fiber bends of 1.5-in. radius
- front access for all cabling and maintenance activities
- retractable doors for cable protection
- covers for cable trough areas
- compatibility with DMS earthquake anchors and systems:
  - — earthquake-designed frame
  - — earthquake anchors
  - — earthquake bracing frames
- compatibility with overhead and under-floor DMS cabling systems
- Bellcore standards for electrostatic discharge (ESD) protection (ESD grounding is not required)

Components

As shown in the following figure, the NTLX91BA DMS frame assembly contains the following SPM equipment and component assemblies:

- NTLX51BA dual-shelf assembly
- NTLX57AA power cabling interface unit (PCIU)
- NTLX5015 air filter
- NTLX5010 upper grill
- NTLX5011 lower grill

NTLX91BA SPM-DMS frame assembly (continued)

- NTLX55AA forced-air cooling unit
- NT0X25BE gray framework

NTLX51AA dual-shelf assembly

One dual-shelf assembly provides 30 slots for the SPM plug-in modules. There are two NTLX51AA dual-shelf assemblies in each NTLX50AA gray framework assembly.

The NTLX51AA dual-shelf assembly accommodates the following items:

- NTLX5201 double-height backplane assembly
- NTLX5101 SPM shelf mechanical assembly (one for each dual-shelf assembly)
- NTLX5016 air-filter tray assembly
- NTLX5102 shelf-door kit
- NTLX5104 shelf cable-trough cover assembly

NTLX51BA dual-shelf assembly

One dual-shelf assembly provides 30 slots for the SPM plug-in modules. There are two NTLX51BA dual-shelf assemblies in each NTLX91BA gray framework assembly.

The NTLX51BA dual-shelf assembly accommodates the following items:

- NTLX5211 double-height backplane assembly
- NTLX5101 SPM shelf mechanical assembly (one for each dual-shelf assembly)
- NTLX5016 air-filter tray assembly
- NTLX5102 shelf-door kit
- NTLX5104 shelf cable-trough cover assembly

NTLX57AA PCIU assembly

The PCIU assembly accommodates a maximum of eight #6 AWG power cables from the power distribution center and 16 #10 AWG power cables for the termination of the shelf power supplies, as well as the required A and B returns.

NTLX91BA SPM-DMS frame assembly (continued)

The NTLX57AA PCIU assembly contains the following items:

- NTLX58AA alarm card assembly (one alarm card for each PCIU assembly)
- NTLX59AA fan management unit assembly (two fan management units for each PCIU assembly)

NTLX5015 air filter assembly

The air filter assembly filters the air supply for the NTLX51BA dual-shelf assembly. There are two NTLX5015 air-filter assemblies for each NT0X25BE gray framework assembly. The air-filter foam-element replacement part-number is A0665487.

NTLX5010 upper grill assembly

The upper grill assembly is located mid-point on the framework assembly. There is one NTLX5010 upper grill assembly for each NT0X25BE gray framework assembly.

NTLX5011 lower grill assembly

The lower grill assembly is located at the bottom of the framework assembly. There is one NTLX5011 lower grill assembly for each NT0X25BE gray framework assembly.

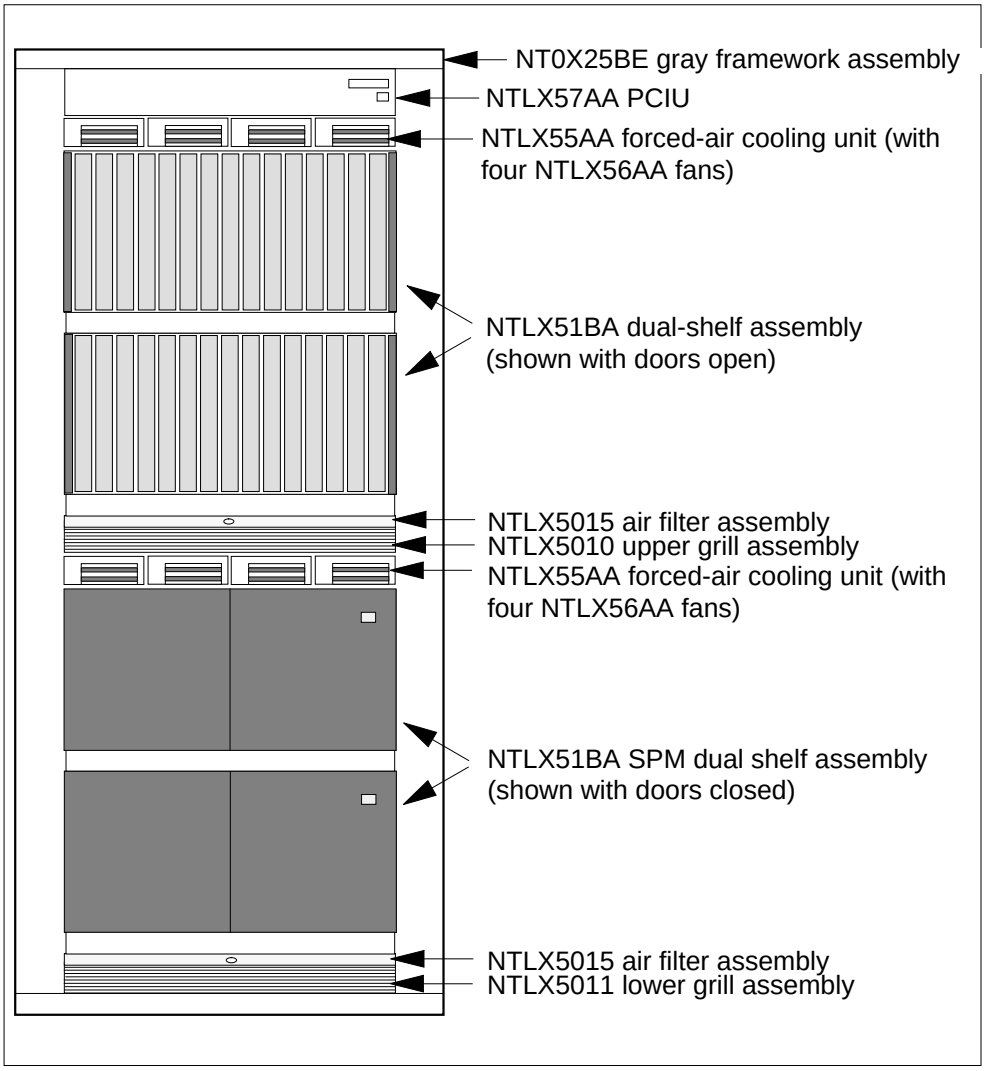
NTLX55AA cooling unit assembly

The cooling unit assembly provides mechanical ventilation for each NTLX51BA dual-shelf assembly. Each NTLX55AA cooling unit assembly contains four NTLX56AA fan assemblies.

NT0X25BE gray framework assembly

The NT0X25BE gray framework assembly consists of the frame that contains the built-in cable ducts, covers, and provides support for all the SPM components. There is one NT0X25BE gray framework assembly for two SPM nodes.

NTLX91BA SPM-DMS frame assembly (continued)



Frame cabling

All the external frame cabling and all inter-assembly internal frame cabling is accessible from the front of the NTLX50BE frame assembly.

NTLX91BA SPM-DMS frame assembly (continued)

Inter-assembly internal frame cabling

The cables listed in the following table connect the assemblies contained in the NTLX91BA frame.

Function	PEC	Connects	To
PCIU to SIM 1	NTLX5094	NTLX57AA PCIU	NTLX61AA SIM on the lower section of the bottom shelf
PCIU to SIM 2	NTLX5095	NTLX57AA PCIU	NTLX61AA SIM on the upper section of the bottom shelf
PCIU to SIM 3	NTLX5096	NTLX57AA PCIU	NTLX61AA SIM on the lower section of the top shelf
PCIU to SIM 4	NTLX5097	NTLX57AA PCIU	NTLX61AA SIM on the upper section of the top shelf
PCIU to cooling unit number 1	NTLX5098	NTLX57AA PCIU	NTLX55AA lower cooling unit assembly
PCIU to cooling unit number 2	NTLX5099	NTLX57AA PCIU	NTLX55AA upper cooling unit assembly
Frame ground cable	NTRX1650	NTLX91BA	Ground

External frame cabling

The external cables listed in the following table connect the NTLX91BA frame to other devices.

(Sheet 1 of 2)

Function	PEC	Number shown in figure	Number of cables	Wire type	Destination
-48 V dc and -48 V dc return	NPS9508-03-6	1	8	#6 AWG	Power distribution cabinet (PDC)
Alarm battery supply	NPS9508-03-14	2	1	#14 AWG	Next frame
Note: The NTLX81AA Fiber Adapter Kit is shipped loose—one kit for each OC3 module.					

NTLX91BA SPM-DMS frame assembly (continued)

(Sheet 2 of 2)

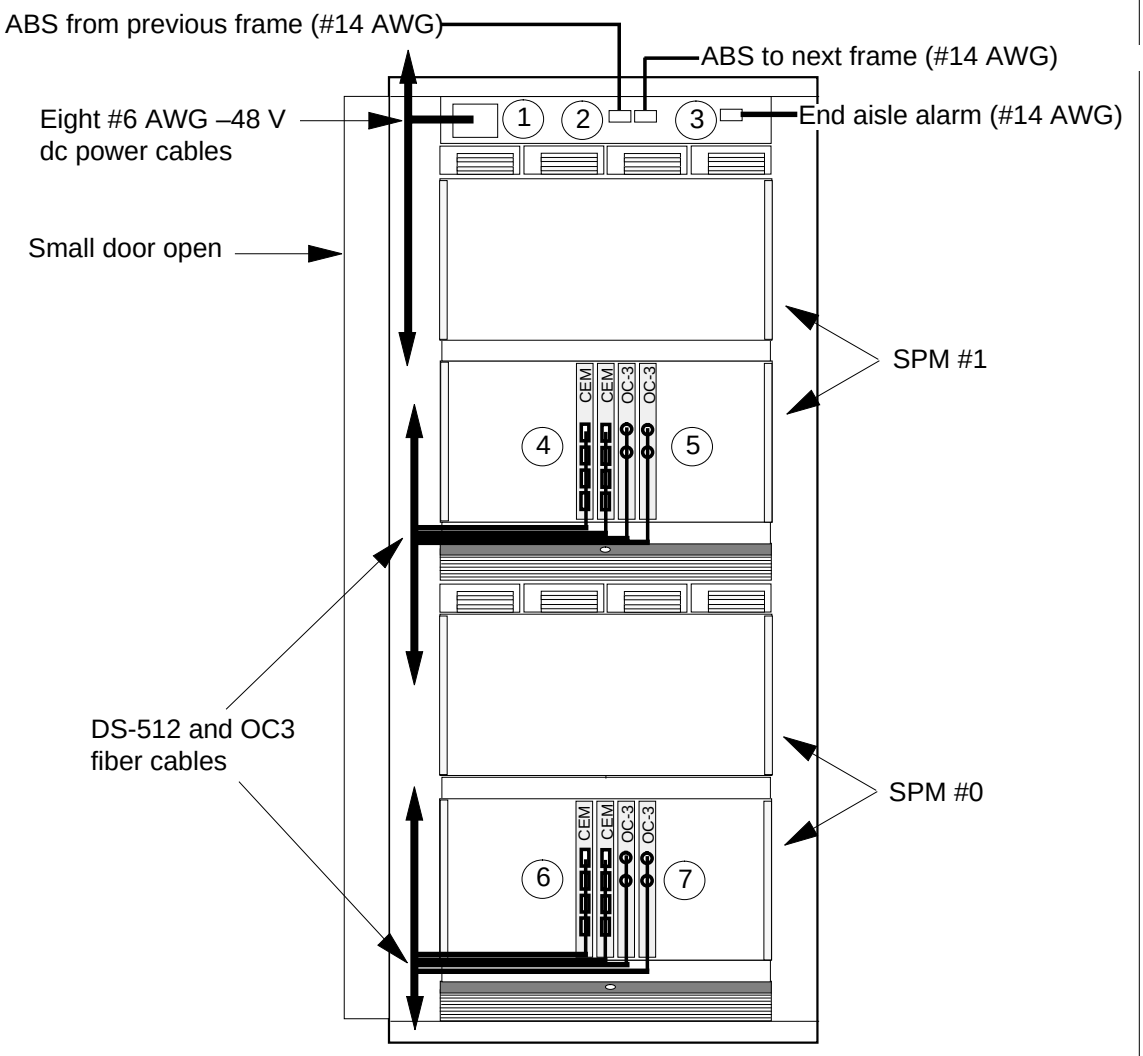
Function	PEC	Number shown in figure	Number of cables	Wire type	Destination
End aisle alarm cable	NT0X96LX	3	1	multiple	End aisle alarm panel (if required)
SPM frame to SPM frame	NT0X96LS	not shown	1	multiple	Next SPM frame (if required)
SPM frame to DTCI frame	NT0X96LQ	not shown	1	multiple	Digital trunk controller ISDN (DTCI) frame (if required)
SPM frame to MSP frame	NT0X96LR	not shown	1	multiple	Modular support panel (MSP) frame
SPM frame to AXU	NT0X96LT	not shown	1	multiple	Alarm cross-connect unit (AXU)
DS-512 from SPM #1	NTLO97AW	4	4	HCS fiber	ENET
OC3 from SPM #1	NTLX81AA	5	4	Fiber adapter kit	Fiber manager
DS-512 from SPM #0	NTLO97AW	6	4	HCS fiber	ENET
OC3 from SPM #0	NTLX81AA	7	4	Fiber adapter kit	Fiber manager

Note: The NTLX81AA Fiber Adapter Kit is shipped loose—one kit for each OC3 module.

Cabling layout

The following figure shows the cabling layout.

NTLX91BA SPM-DMS frame assembly (continued)

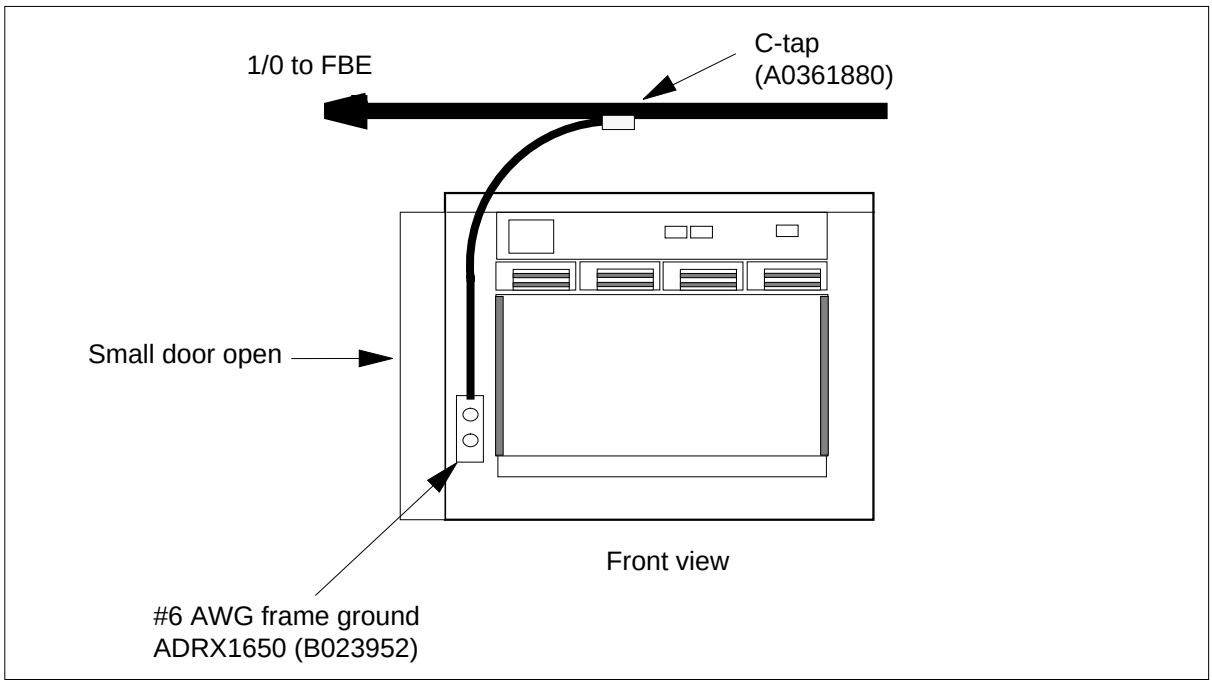


Note: Fiber, alarm, and power cables can be routed up to cable racks or down to the raised floor.

NTLX91BA SPM-DMS frame assembly (continued)

Frame ground

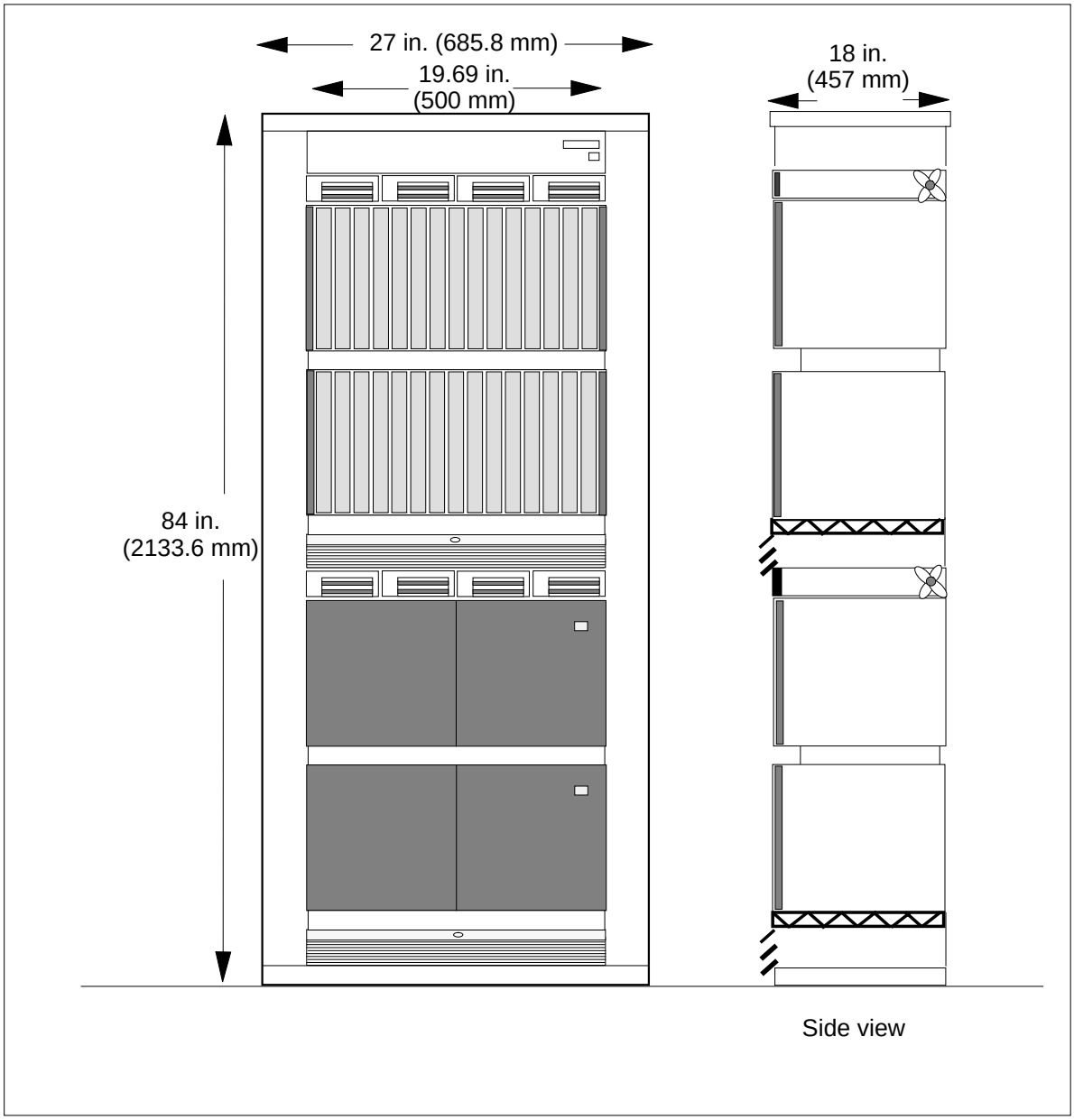
The following figure shows the #6 AWG frame ground connection mounted on the left front of the NTLX91BA frame assembly. The frame ground cable requires a C-tap to a 1/0 cable connected to the frame bonding equalizer (FBE) and routed in the cable trough throughout the length of the frame line up.



Frame design

For the North American market, SPM installs in a DMS frame that measures 7 ft (2133.6 mm) x 2.25 ft (457 mm) x 1.5 ft (457 mm). The following figure shows the NTLX91BA DMS frame dimensions.

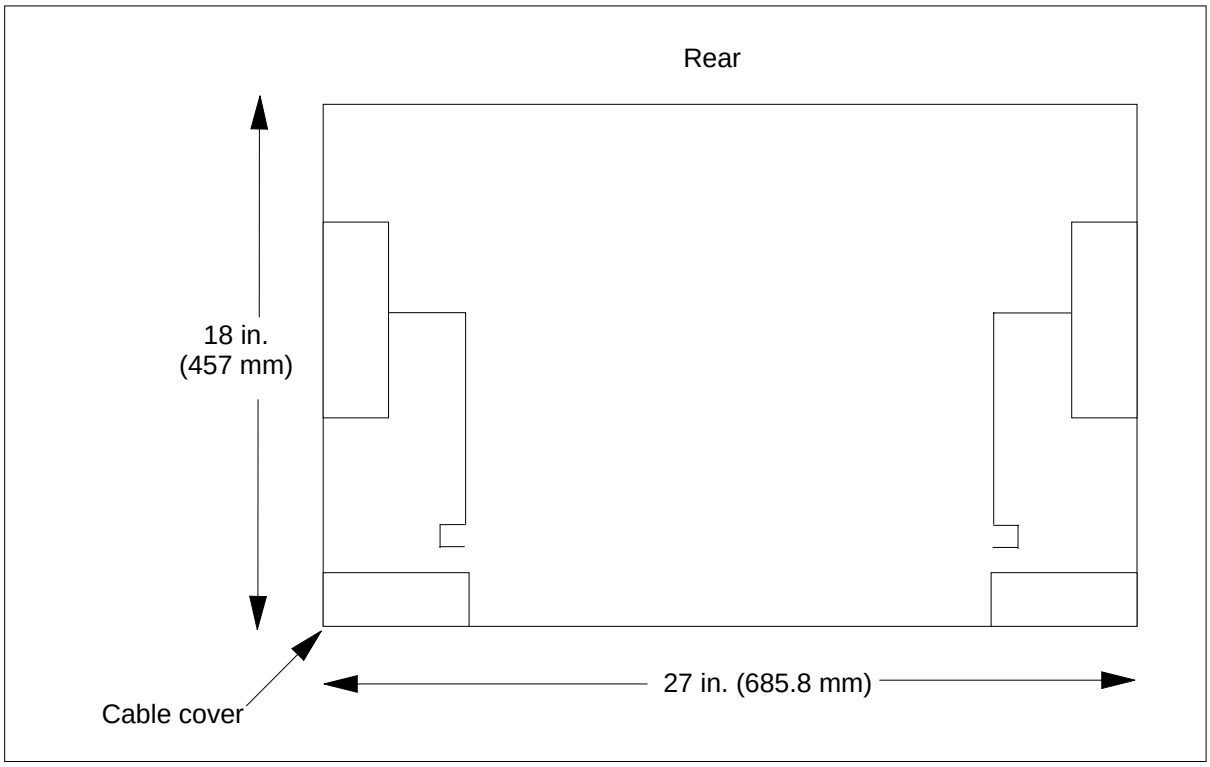
NTLX91BA SPM-DMS frame assembly (continued)



Floor footprint

The following figure shows the footprint of a NTLX91BA DMS frame. The NTLX91BA frame is capable of housing two SPM nodes in this area.

NTLX91BA SPM-DMS frame assembly (end)



List of terms

ABH or ABBH
A/B bit handler

ABS
alarm battery supply

ALM
alarm unit

application-specific integrated circuit
An integrated circuit designed for a specific application process.

ASIC
See application-specific integrated circuit.

AWG
American Wire Gauge

AXU
alarm cross-connect unit

BDM
bit demodulator

BWA
bandwidth allocator

CCS7
See Common Channel Signaling System 7.

CEM
common equipment module

CI
See command interpreter.

circuit pack

In DMS-Supernode, consists of multilayer printed circuit board, through-hole electronic components, backplane connector, faceplate, lock latches, and stiffeners.

CM

See computing module.

command interpreter

A support operating system component that functions as the main interface between machine and user. Its principal roles are to read lines entered by a terminal user, to break each line into recognizable units, to analyze the units, to recognize command item-numbers on the input lines, and to invoke these commands.

Common Channel Signaling 7

A digital, message-based network signaling standard defined by the CCITT that separates call signaling information from voice channels so that interoffice signaling is exchanged over a separate signaling link.

computing module

The processor and memory of the dual-plane combined core used by the DMS SuperNode switch. It coordinates call processing functions of the switch, including the actions of the network and peripheral modules. Each computing module consists of a pair of central processing units with associated memory that operate in a synchronous matched mode on two separate planes. Only one plane is active; it maintains overall control of the system while the other plane is on standby.

controlled sparing

A type of sparing action that occurs if the operating company personnel indicates, by way of a MAP interface, that a deload of the resource module is appropriate. The non-restorable resources on the resource module are deloaded before the resource modules are spared.

COT

continuity tone transceiver

CP

See circuit pack. Also called a printed circuit pack.

CPU

central processing unit

CRC

See cyclic redundancy check.

CSM

channel supervision and messaging

cyclic redundancy check

A method of detecting errors. Typically a 16-bit check character is added to each data block based on a repeated examination of each information bit.

DLC

See digital link controller.

digital link controller

Resource module used in call processing on an SPM.

digital signal processor

Software that runs on the service test head analog board, which is used to perform line card testing and subscriber loop diagnostics.

digital trunk controller

A peripheral module that connects DS-30 links from the network to digital trunk circuits.

DMS

Digital multiplex system. Telephone switching equipment, namely, digital switching units for interconnecting telephone subscribers, and control terminals. A Nortel trademark.

DMS-100 switch

A Nortel trademark for specific telephone switching equipment.

DMS SuperNode

A central control complex for the DMS Family. The two major components of DMS SuperNode are the computing module and the message switch. Both are compatible with the DMS Family network module, the input/output controller, and the XMS-based peripheral modules.

DRAM

See dynamic random access memory.

DSP

See digital signal processor.

DSPI

DSP island

DTC

See digital trunk controller.

DTCI

digital trunk controller island

DTMF

See dual-tone multifrequency.

dual-tone multifrequency

A signaling method that uses set combinations of two specific voice-band frequencies. One of these voice-band frequencies is selected from a group of four low frequencies, and the other is selected from a group of three or four relatively high frequencies.

dynamic random-access memory

A random access memory system that employs transistor capacitor storage cells. The logic state is stored in the capacitor and buffered by the transistor. The capacitive charge must be refreshed at a periodic rate to maintain its programmed state.

ECAN

echo canceller

electromagnetic interference

The radiated and conducted energy from digital electronic equipment that may interfere with radio transmission.

EMC

electro-magnetic capability

EMI

See electromagnetic interference.

ENET

See enhanced network.

ESD

electrostatic discharge

enhanced network

Channel-matrixed time switch that provides pulse code modulated voice and data connections between peripheral modules. It also provides message paths to the DMS-bus components.

FBE

frame bonding equalizer

FDL

facility data link

FMU

fan management unit

h-CPS

half-calls per second

HCS

hard-clad silica

ICM

integrated connection memory

Integrated Services Digital Network

A set of standards proposed by the CCITT to establish compatibility between the telephone network and various data terminals and devices. ISDN is a fully digital network. It provides end-to-end connectivity to support a wide range of services including circuit-switched voice, circuit-switched data, and packet-switched data over the same local facility.

ISDN

See Integrated Services Digital Network.

ISDN User Part

A Common Channel Signaling 7 message-based signaling protocol that acts as a transport carrier for ISDN services. It provides the functionality in a CCS7 network for voice and data services.

ISUP

See ISDN User Part.

ITM

intelligent test bus master

MAP

A Nortel trademark for testing and maintenance center for operating company switching equipment Examples of the correct use are *MAP terminal* or *MAP workstation.*

MAPCI

See MAP Command Interpreter.

MAP Command Interpreter

A MAP level for accessing maintenance and other functional levels.

MAP terminal or workstation

The maintenance and administration position. It is a group of components that provide a user interface between operating company personnel and the

DMS Family systems. It consists of a visual display unit and keyboard, a voice communications module, test facilities, and MAP furniture. MAP is a trademark of Nortel.

MF

See multifrequency.

MIM

module information memory

MSP

modular support panel

multifrequency

A signaling method that makes use of pairs of standard tones to transmit signaling codes, digit pulsing, and coin-control signals. This method is used in interregister signaling on analog trunks.

Nortel Publication

A technical document that is intended to assist operating company personnel with the operations, administration, maintenance, and provisioning of Nortel products, including both hardware and software. NTPs contain descriptive and procedural information. They are usually supplied to an operating company as part of the purchased product.

NTP

See Nortel Publication.

OAM or OA&M

See operations, administration, and maintenance.

OAM&P

operations, administration, maintenance, and processing

OC

optical carrier

OC3

optical carrier 3

OMaR

octal mapping resource

operations, administration, and maintenance

All the tasks necessary for providing, maintaining, or modifying the services provided by a switching system. These tasks include provisioning

of hardware, creation of service, verification of new service, and trouble recognition and clearance.

PCIU

power cabling interface unit

PCP

printed circuit pack. See circuit pack.

PDC

power distribution center

PEC

See product engineering code.

per-trunk signaling

A conventional telephony method of signaling that multiplexes the control signal of a call with voice or data over the same trunk.

peripheral module

A generic term referring to all hardware modules of the DMS Family systems that provide interfaces with external line, trunk, or service facilities. The peripheral module contains peripheral processors that perform local routines, thus relieving the load on the central processing unit.

PLL

phase lock loop

PM

See peripheral module.

point-of-use power supply

The type of power supply for an enhanced line concentrating module.

PRBS

pseudo-random bit sequencing

product engineering code

An eight-character unique identifier for each marketable hardware item manufactured by Nortel.

PRSU

post-release software update

PTS

See per-trunk signaling.

PUPS

See point-of-use power supply.

QLC

quad link controller

RAM

See random access memory.

random access memory

A static read/write memory system in which information is stored in discrete individually addressable locations such that access time is independent of location.

read-only memory

A solid state storage chip that is programmed at the time of its manufacture and that cannot be reprogrammed by the computer user.

resource module

A software module that performs packet switching operations on data packets sent from the access module or from digital trunks in the packet switched network.

RM

See resource module.

RMan

resource management

ROM

See read-only memory,

SDH

synchronous digital hierarchy

Signaling System 7

A version of signaling system #7 that was developed for North American use.

SIM

shelf interface module

SLIF-M

serial link interface-master

SLIF-S

serial link interface-slave

S-link

serial link

SONET

See synchronous optical network.

SPE

synchronous payload envelope

Spectrum node

A Spectrum node consists of the components on the two shelves connected to an optical carrier network by a pair of OC-3 modules. Two Spectrum nodes can be contained in a single Spectrum frame.

Spectrum system

The term used to refer the Spectrum telecommunications platform in general terms, without refering directly to any individual component or group of components.

SPM

A short form designator for the Spectrum system, which is used in the DMS MAPCI interface. SPM can also mean Spectrum peripheral module, when used in a DMS context.

SS7

See Signaling System 7.

STS

synchronous transport signal

SuperNode

Central control complex for the DMS-100 Family switch. The two major components of DMS SuperNode are DMS-Core and DMS-Bus. DMS-Bus consists of dual message switch (MS) shelves; DMS-core consists of a computing module shelf and a system load module. Nortel trademark.

SWACT

See switch of activity.

switch of activity

1) Activity switch between CPUs for maintenance purposes.

2) In a DMS fault-tolerant system, a reversal of the states of two identical devices devoted to the same function. A SWACT makes an active device inactive and an inactive device active.

synchronous optical network

A standard for optical transport that defines optical carrier levels and their electrically equivalent synchronous transport signals. The SONET standard allows for a multivendor environment, positioning of the network for transport of new services, synchronous network, and enhanced operation, administration, and maintenance.

tDSPI

turbo digital signal processing island

TONESYN

Tone Synthesizer

VCXO

voltage controlled crystal oscillator

VSP

voice signal processor

VSP RM

voice signal processor resource module

VT

virtual tributary

XPT

crosspoint card

Digital Switching Systems

DMS-Spectrum Peripheral Module

Hardware Maintenance Reference Manual

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